

Abstract Title: (Study of Metallization-Induced Interface Traps and Charge in $\text{Al}_2\text{O}_3/\text{SiO}_2/\text{Si}$ MOS Stack Using C–V/G–V Measurements and TCAD Simulations)

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Abstract

Atomic layer deposited (ALD) Al_2O_3 on thermally grown SiO_2 as a bilayer stack is emerging as a robust gate dielectric and passivation layer for low-power CMOS, high-power devices, embedded non-volatile memories, emerging 2D-FET, and PERC solar cells. Because post-deposition annealing (PDA) can damage fragile channel interfaces or exceed the thermal budget of back-end and 3D-sequential integration, the critical bottleneck is the integration of the metal electrode after the dielectric deposition. In this study, we fabricate $\text{Al}_2\text{O}_3/\text{SiO}_2/\text{Si}$ metal-oxide semiconductor (MOS) structures using three different metallization methods, such as thermal evaporator, e-beam evaporation, and sputtering. Using the capacitance-voltage (C-V) measurement technique, we extract and compare the effective oxide-trapped charges (Q_{eff}) and interface trap states (N_{eff}) of samples whose electrodes were deposited using the three methods. Thermal evaporation was found to be the most optimal method, producing the lowest effective oxide charge ($(9.4 \pm 0.2) \times 10^{10} \text{ cm}^{-2}$) and N_{eff} ($(6.6 \pm 0.5) \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) in the stack. Sputtered metallization resulted in the highest effective oxide charge ($(6.2 \pm 0.5) \times 10^{12} \text{ cm}^{-2}$) and significant border trap charge (Q_{bt}). Notably, the e-beam method also generated high and nearly equal N_{eff} ($\sim 1.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$), indicating high near-interface damage. TCAD simulation fitting to experimental C-V data yielded a unique trap distribution. PMA helps in a significant reduction of generated trap charges, but does not remove them completely. Hence, there is a residual effect of the high-energy metallization method on the $\text{Al}_2\text{O}_3/\text{SiO}_2/\text{Si}$ stack that must be considered in semiconductor design and manufacturing.

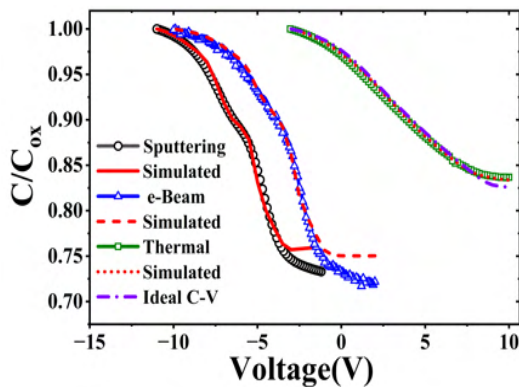


Fig.1 Measured and simulated C-V characteristics of as-deposited stack at frequency 50 kHz metallized by sputtering, e-beam, and thermal techniques.

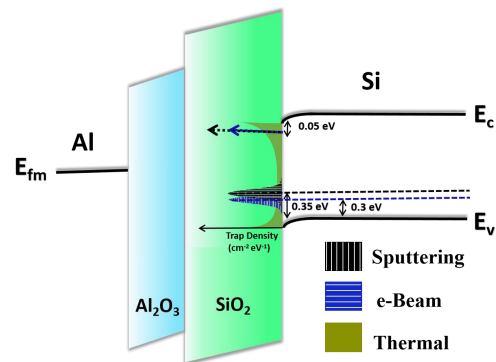


Fig.2 Energy band diagram with predicted trap distribution profile using TCAD simulations.