PCSI

Room Ballroom - Session PCSI-MoE

High-k Dielectrics & Devices Interfaces

Moderator: Xia Hong, University of Nebraska - Lincoln

7:30pm **PCSI-MoE-1 UPGRADED: Time Evolution of Surface Chemical Reactions During Aluminum Oxide Atomic Layer Deposition on InAs**, *Rainer Timm, **Eleni Charitoudi**, Nishant Patel,* Lund University, Sweden*; Rosemary Jones, Esko Kokkonen,* Max IV Laboratory, Sweden

III-V semiconductors have highly promising properties for electronic applications. Specifically, InAs has a narrow, direct band gap and high electron mobility, making it a good candidate to outperform Si-based Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) in terms of speed and power consumption. The detrimental native oxide should thereby be replaced by a so-called high-k oxide, such as Al_2O_3, improving the gate properties. However, the performance of this system is limited by a high defect density at the InAs/Al_2O_3 interface,[1] which is attributed to the incomplete removal of the native oxide layer.

The precise deposition of Al_2O_3 on InAs is achieved via atomic layer deposition (ALD), enabling the production of thin films with atomic-scale precision. It is characterised by a layer-by-layer mechanism and the self-limiting interaction between two gaseous precursors and the substrate. In our case, two half-cycle depositions were performed using trimethylaluminum (TMA) and water as precursors. A common method for studying the chemical composition and interface quality of ALD films is to perform X-ray photoelectron spectroscopy (XPS) measurements before and after each half-cycle. Here, we instead use ambient-pressure XPS (AP-XPS) to monitor time-resolved surface chemical reactions during ALD half-cycles in the implemented ALD cell at the SPECIES synchrotron beamline of the MAX IV Laboratory.[2]

Upon ALD, the As-oxide was found to get entirely removed during the initial TMA half-cycle (TMA), as shown in **Figure 1** (supplemental document). This self-cleaning is far less efficient for the In-oxide, which only decreases slightly in intensity. More interestingly, the type of In-suboxide changes upon ALD, resulting in a decreased In oxidation state after TMA deposition and an increased oxidation state after water pulsing. Such a re-oxidation of the substrate material upon ALD, in parallel with the wanted formation of Al_2O_3, is unexpected, and it is in contrast with previous results from AP-XPS measurements of HfO_2 ALD on InAs.[3,4] Here, we will compare the two high-k ALD processes based on reaction dynamics observed from time-resolved In, As, Al, Hf, and C core-level spectra, including different organic ligands and reaction byproducts.

References:

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2. Kokkonen, E. et al., Journal of Synchrotron Radiation 28, 588–601 (2021).

3. D'Acunto, G. et al., ACS Applied Electronic Materials 2, 3915–3922 (2020).

4. D'Acunto, G. et al., Surfaces and Interfaces 39, 102927 (2023)

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7:45pm **PCSI-MoE-4 Direct Evaluation of SiO_2/Al_2O_3 Interface Dipole for $Si/SiO_2/Al_2O_3/HfO_2$ Gate Stack Using Operando HAXPES**, ***Masaki Ando***, Meiji University, Japan*; Takashi Onaya, Toshihide Nabatame,* National Institute for Materials Science (NIMS), Japan*; Satoshi Toyoda,* Office of Institutional Advancement and Communications, Kyoto University, Japan*; Atsushi Ogura,* Meiji University, Japan

Background: Dipole techniques have been investigated to control the threshold voltage (V_t) in n- and p-FETs, and Al_2O_3 has been proposed as a candidate dipole material for p-FETs [1,2]. An Al_2O_3 dipole layer is inserted at the SiO_2/HfO_2 interface of $Si/SiO_2/HfO_2$ gate stacks, and its thickness is controlled by the number of atomic layer deposition (ALD) cycles. V_t is known to be affected by both fixed charges and dipoles in the gate stack; however, it has been difficult to separate them by electrical measurements. In this study, we directly evaluate the SiO_2/Al_2O_3 interface dipole in $Si/SiO_2/Al_2O_3/HfO_2$ stacks using hard X-ray photoelectron spectroscopy under gate bias (operando HAXPES) [3].

Experiment: Al/p-Si/SiO_2(9 nm)/Al_2O_3(0 or 0.2 nm)/HfO_2(4 nm)/Pt stacks were prepared using ALD. Using operando HAXPES at SPring-8 BL46XU (hv = 7.94 keV, $|V_g| \leq 1.5$ V), Hf 3d, Si 1s and Pt 3d spectra were acquired while applying a gate voltage [Fig. 1(a)]. As each core level follows its layer's potential, sep_c = BE(Si 1s (Si^{4+})) - BE(Hf $3d_{5/2}$) gives the HfO_2-SiO_2 potential difference across Al_2O_3. The measured interface dipole was corrected as sep_c reflects only 60% of the actual value due to a 40% V_g drop between Hf 3d and Si^{4+}.

Results: The Al_2O_3-induced change in sep_c was 0.14 ± 0.03 eV after correction for the V_g drop [Fig. 1(b)]. This actual interface dipole was independent of V_g and polarity [Fig. 1(b),(c)], excluding the possible influence of mobile ions and charge trapping. The sep_c of the 0.4-nm-thick Al_2O_3 sample was almost the same due to saturation of the dipole effect (data not shown). Both the corrected sep_c value and saturation trend are consistent with reported C-V results (V_{fb} shift of +0.14 to +0.25 V) [4]. Thus, operando HAXPES is a promising analysis method to evaluate the SiO_2/Al_2O_3 interface dipole under gate bias.

[1] K. Iwamoto et al., Appl. Phys. Lett. 92, 132907 (2008).

[2] J. Yao et al., IEDM Tech. Dig. 2022, 34.2.1.

[3] Y. Yamashita et al., J. Appl. Phys. 115, 043721 (2014).

[4] T. Nabatame et al., 73rd JSAP Spring Meeting (2026).

7:50pm **PCSI-MoE-5 How to Choose a Gate Dielectric for Rutile GeO_2**, ***Xiaoru Zhang***, The University of Texas at Austin*; Alexander A. Demkov,* University of Texas at Austin

Electrification, renewable-energy conversion, and data-intensive computing require efficient power electronics at high voltage, frequency, and temperature. Wide-bandgap semiconductors address these needs, while ultrawide-bandgap (UWBG) materials offer still larger breakdown fields [1]. Rutile GeO_2 (r-GeO_2) is an emerging UWBG semiconductor with a ≈4.7 eV gap, favorable thermal transport properties, predicted possibility of ambipolar doping, and recent demonstration of single-crystal growth and fabrication of MOSFET [2,3,4]. However, metal–oxide–semiconductor devices require structurally compatible gate dielectrics with sufficiently large barriers to both electron and hole injection. Because r-GeO_2 has a rather wide gap, satisfying both barrier conditions is especially restrictive [5].

We use first-principles calculations to compare r-GeO_2(001) interfaces with crystalline and amorphous SiO_2, crystalline and amorphous Al_2O_3, and crystalline MgO. Amorphous oxides are generated by melt-and-quench molecular dynamics, and representative atomistic models are shown in Fig. 1. Valence-band offsets are independently determined from core-level alignment, electrostatic-potential lineups, and layer-projected densities of states. The conduction-band offsets are then determined using experimental band gaps for dielectrics and ab initio band gaps for r- GeO_2. All five interfaces exhibit type-I band alignment. MgO and Al_2O_3 show asymmetric carrier confinement, with relatively large electron barriers but comparatively weak hole barriers. SiO_2 provides the most balanced confinement for both carrier types.

[1] J. Y. Tsao et al., Adv. Electron. Mater. 4, 1600501 (2018). [2] S. Chae et al., Appl. Phys. Lett. 114, 102104 (2019); [3] P. Emtenani et al., Adv. Funct. Mater. 36, e76723 (2026); [4] K. Tetzner et al., IEEE Electron Device Lett. 47, 566 (2026). [5] J. Robertson, J. Non-Cryst. Solids 303, 94 (2002).

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7:55pm **PCSI-MoE-6 Study of Metallization-Induced Interface Traps and Charge in Al2O3/SiO2/Si MOS Stack Using C–V/G–V Measurements and TCAD Simulations**, ***Swadhin Jena***, *Akshay K., Parlapalli Satyam,* IIT Bhubaneswar, India

Atomic layer deposited (ALD) Al_2O_3 on thermally grown SiO_2 as a bilayer stack is emerging as a robust gate dielectric and passivation layer for low-power CMOS, high-power devices, embedded non-volatile memories, emerging 2D-FETs, and PERC solar cells. Because post-deposition annealing (PDA) can damage fragile channel interfaces or exceed the thermal budget of back-end and 3D-sequential integration, the critical bottleneck is the integration of the metal electrode after the dielectric deposition. In this study, we fabricate $Al_2O_3/SiO_2/Si$ metal-oxide semiconductor (MOS) structures using three different metallization methods, such as thermal evaporation, e-beam evaporation, and sputtering. Using the capacitance-voltage (C-V) measurement technique, we extract and compare the effective oxide-trapped charges (Q_{eff}) and interface trap states (N_{eff}) of samples whose electrodes were deposited using the three methods. Thermal evaporation was found to be the most optimal method, producing the lowest effective oxide charge ((9.4 ± 0.2) ×10^{10} cm^{-2}) and N_{eff} ((6.6 ± 0.5) × 10^{11} cm^{-2} eV^{-1}) in the stack. Sputtered metallization resulted in the highest effective oxide charge ((6.2 ± 0.5) ×10^{12} cm^{-2}) and significant border trap charge (Q_{bt}). Notably, the e-beam method also generated high and nearly equal N_{eff}(~ 1.5 × 10^{12} cm^{-2} eV^{-1}), indicating high near-interface damage. TCAD simulation fitting to experimental C-V data yielded a unique trap

distribution. PMA helps in a significant reduction of generated trap charges, but does not remove them completely. Hence, there is a residual effect of the high-energy metallization method on the $Al_2O_3/SiO_2/Si$ stack that must be considered in semiconductor design and manufacturing.

8:00pm **PCSI-MoE-7 Influence of Ti Adhesion Layer and ALD Al2O3 Thickness on Metal/Insulator/Metal (MIM) Interfacial Energy Barriers***, **John Conley**, Jessica Haglund,* Oregon State University

Understanding and control of interfacial energy barriers (ϕBn's) at metal/insulator contacts is essential for designing MIM and MOS based devices. Interfacial energy barriers are difficult to predict as they depend not only on the metals and dielectrics used, but also on deposition method, deposition order, interfacial interactions such as diffusion and oxygen scavenging, intrinsic and extrinsic defects, and possibly even film thickness. Ultrathin dielectrics are needed for MOS gates and MIM capacitors. It has been reported that the dielectric constant, density, and optical refractive index of ALD Al2O3 are a function of film thickness. Thin interfacial metals have been investigated to tailor barrier heights and are required for good adhesion of noble metal electrodes to oxides. In this work, we investigate the impact of Ti adhesion layer (dTi) and Al2O3 film (dAl2O3) thickness on ϕBn's in bimetal electrode Pt/Ti/Al2O3/TiN MIM devices using internal photoemission (IPE) spectroscopy.

100 nm TiN bottom electrodes were reactive ion sputtered. Al2O3 was then deposited via ALD at 250 ˚C using TMA / H2O in either a Picosun R150 or R200 chamber. Following ALD a thin Ti IL (0.5, 1, 2, 5, 10 nm) and a 10 nm Pt top electrode were deposited via electron beam evaporation using a shadow mask. CV and IV measurements were taken on the MIM structures. Energy barriers were measured using a lab-built IPE spectrometer system.1 Top gate voltage was swept from 0 to +/- 2 V using +/- 0.1 V steps. At each bias, incident photon energy was swept from 1.7 to 5.5 eV. IPE thresholds (ϕthresh) were determined at each voltage using yield plots and zero field barriers (ϕBn) were determined using Schottky plots.

dAl2O3: Impact Both the top Pt/Al2O3 and bottom TiN/Al2O3 electron barriers were found to be a function of dAl2O3. While both barriers were roughly constant at ~3.6 eV for Al2O3 films ≥ 12 nm thick, both decreased by roughly 0.5 eV as dAl2O3 decreased down to 5 nm.

dTi: For bimetal Pt/Ti electrodes, a 0.5 to 1.0 nm thick interfacial Ti layer was found sufficient to completely dominate the barrier with Al2O3. Insertion of the Ti layer resulted in band tailing at the top interface, likely due to oxygen scavenging, but had no impact on the bottom Al2O3/TiN barrier.

The degradation of interfacial energy barriers with Al2O3 thickness and the dominant influence of even a very thin Ti interfacial layer on ϕBn are important considerations for the prediction and optimization of leakage currents and performance for these devices.

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8:05pm **PCSI-MoE-8 Consistency Checks for Semiconductor Contact Extraction***, **Dong Kyun Lim**, Jin-Hong Park,* Sungkyunkwan University (SKKU), Republic of Korea

Finite-length transmission-line model (TLM) fits can return positive contact parameters despite uncertain geometry or incorrect de-embedding. We present an explicit consistency workflow for extracting specific contact resistivity and under-contact sheet resistance within established finite-contact TLM. For positive, width-normalized, de-embedded contact-front resistances Q1 and Q2 at effective lengths L1 and L2, uniform linear-ohmic, one-dimensional transport with equipotential metal and shared positive contact parameters implies $1 < r < k$, where $r = Q1/Q2$ and $k = L2/L1 > 1$.

A joint (r,k) uncertainty region is screened before inversion. Disjointness from the closed admissible domain indicates inconsistency with the combined model and error assumptions; boundary overlap is inconclusive; a strictly interior region permits conditional inversion. Resistance–geometry covariance can reverse classification in either direction relative to a fixed-geometry ablation at the same cutoff. Transfer-length sensitivity deteriorates near both ratio limits.

Across 1,500 synthetic Gaussian regions, the analytical procedure and a same-information constrained-distance solver gave identical decisions. In a selected synthetic de-embedding-offset example, a noiseless two-length fit overestimated specific contact resistivity by 16.4% and under-contact sheet resistance by 45.6%. All 30,000 noisy two-length regions were interior, yet a nominal 95% held-out third-length residual test rejected only 6.90%. The workflow makes conditional extractability and its limits explicit; neither an interior result nor agreement at an additional length validates the physical model. No measured device data or inferential superiority are claimed.

8:10pm **PCSI-MoE-9 Studying Thin Film Surface & Interface Engineering Using Xps and Strataphi: Depth-Resolved, Non-Destructive Analysis of Layered Materials***, **Jia Lu**, Norb Biderman,* Physical Electronics USA

The development of next-generation engineered materials demands new approaches. As material systems become more complex, the need for accurate and precise depth-resolved characterization of layered materials becomes critical for understanding the devices' performance, reliability, and process control. *Strata*PHI 3.0 introduces an integrated characterization platform designed for non-destructive, depth-resolved analysis of multi-layer structures composed of ultra-thin layers.

By leveraging data from X-ray photoelectron spectroscopy (XPS) and hard X-ray photoelectron spectroscopy (HAXPES), *Strata*PHI extracts the key processing-dependent material parameters (e.g. layer thickness, composition, and fractional coverage) across the multi-layer stack, from sub-monolayer up to 30 nm below the surface. The newest *Strata*PHI platform also introduces an "integrated analyzer acceptance angle mode (AAA mode)", further strengthens *Strata*PHI's application in metrology, delivering rapid and reliable thickness measurement using a single take-off angle (TOA).

For ultra-thin films prepared using atomic layer deposition (ALD), the key question is not only how thick the deposited material is, but also how completely it covers the substrate. Traditionally, characterization of fractional coverage of thin films is done by a stand-alone low energy ion scattering (LEIS) instrument for the best sensitivity and peak separation. *Strata*PHI uses XPS peak intensities and attenuation-based thin-film models to simultaneously evaluate thickness and coverage of ALD-deposited layers. *Strata*PHI fraction coverage calculation for Al_2O_3 deposited on SiO2/Si substrate shows similar values compared to the stand-alone LEIS across multiple ALD cycles.

This poster presentation will demonstrate how *Strata*PHI enables researchers, scientists, and engineers to model complex ultra-thin film structures, providing a deep understanding of the ultra-thin films, surfaces, as well as buried interfaces. With automated batch processing, *Strata*PHI can further link processing conditions to thin-film properties, providing a comprehensive characterization suite for tighter control over performance and reliability of new materials and devices.

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