Local deep level transient spectroscopy imaging for MOS interface trap distribution

N. Chinone,[1] and Y. Cho[1]
[1] *Research Institute of Electrical Communication, Tohoku University, Sendai, Japan*

Physical properties of metal-oxide-semiconductor (MOS) interface are critical for semiconductor devices. There are several techniques for characterizing MOS interface properties. Deep level transient spectroscopy (DLTS) [1] is one of powerful techniques capable of macroscopic quantitative evaluation of trap density at/near MOS interface. But it is easily imagined that actual trap is not homogeneously distributed but has two dimensional distributions in atomic scale and even in mesoscopic scale. Therefore, it is very important to characterize MOS interface microscopically. Unfortunately, it is impossible to observe such inhomogeneity by using conventional macroscopic DLTS method.

In this paper, a new technique for local DLTS imaging using scanning nonlinear dielectric microscopy (SNDM) [2] is proposed. This method enables us to observe two dimensional distribution of trap density at/near MOS interface and is demonstrated with oxidized SiC wafer.

We measured three n-type silicon face (4°-off) 4H-SiC wafer samples on which 45-nm-thick thermal silicon dioxide film was formed. Two of them were followed by post oxidation annealing (POA) in nitric oxide ambient with different annealing conditions: (a) 10 min in 1250°C and (b) 60 min in 1150°C. We labeled the samples without POA, with POA in condition (a) and with POA in condition (b) as #S-45-1, #S-45-2 and #S-45-3, respectively. These three samples were scanned on $1.5\times1.5\mu m^2$ square area with a resolution of 30×30 pixels and analyzed using the proposed local DLTS method. By analyzing the acquired images, time-constant and magnitude of transient capacitance response were obtained at each pixel. As shown in Figure 1, highest brightness was obtained from #1 and lowest one was obtained from #3, which is consistent with macroscopically obtained result (#1 sample has highest trap density and #3 sample has lowest one.). Furthermore, in the local DLTS images, we detected dark and bright areas, which can be translated as two dimensional trap distribution. This means that this is the first demonstrations of two dimensional imaging of trap distributions in MOS interfaces.

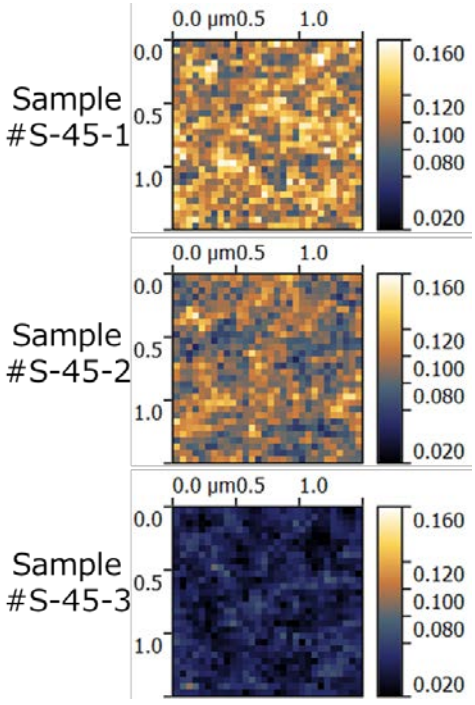

Figure 1. Images of Local-DLTS signal around τ=1μsec of SiC MOS interface. The dark and bright areas are interpreted as low D_{it} (trap density) area and high D_{it} area, respectively.

+ Author for correspondence: yasuocho@riec.tohoku.ac.jp
[1] D. V. Lang: J. Appl. Phys. **45**, 3023 (1974).
[2] Y. Cho et al.: Rev. Sci. Instrum. **67**, 2297(1996).

Suplementary Information

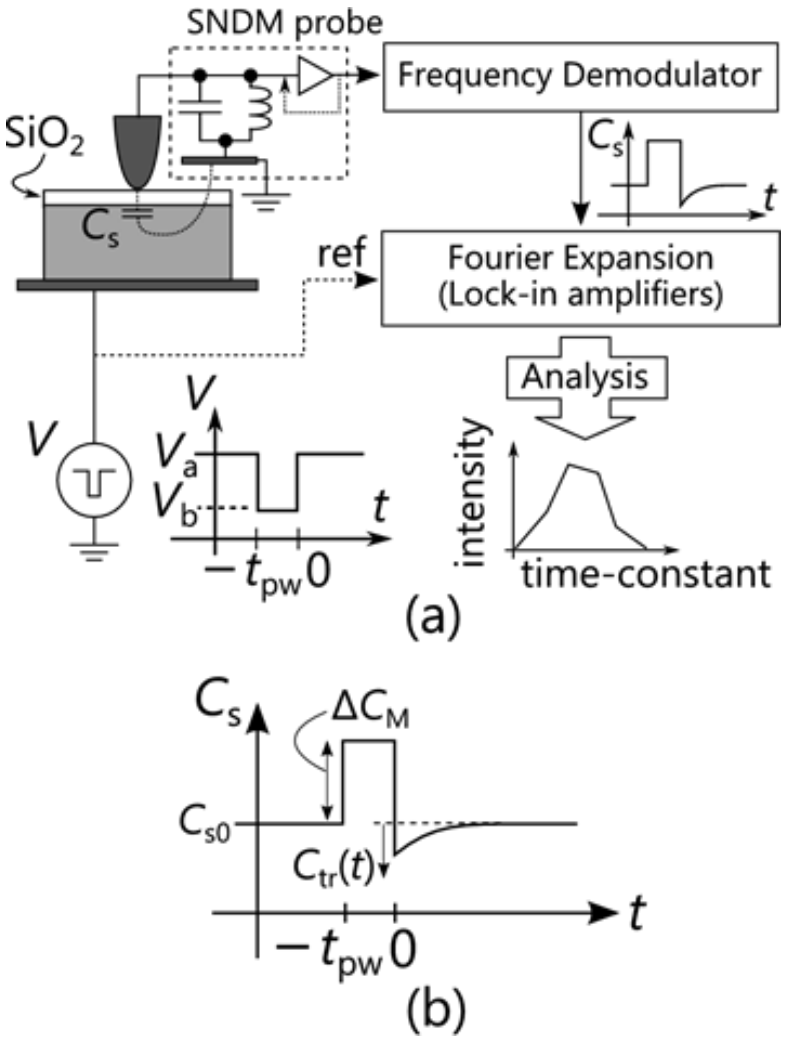

Figure 2. (a) Block diagram of the local DLTS system. (b) The transient capacitance response which is expressed by $C_{tr}(t) = \sum_{k=1}^{Nt} c(\tau_k) \exp(-t/\tau_k)$.

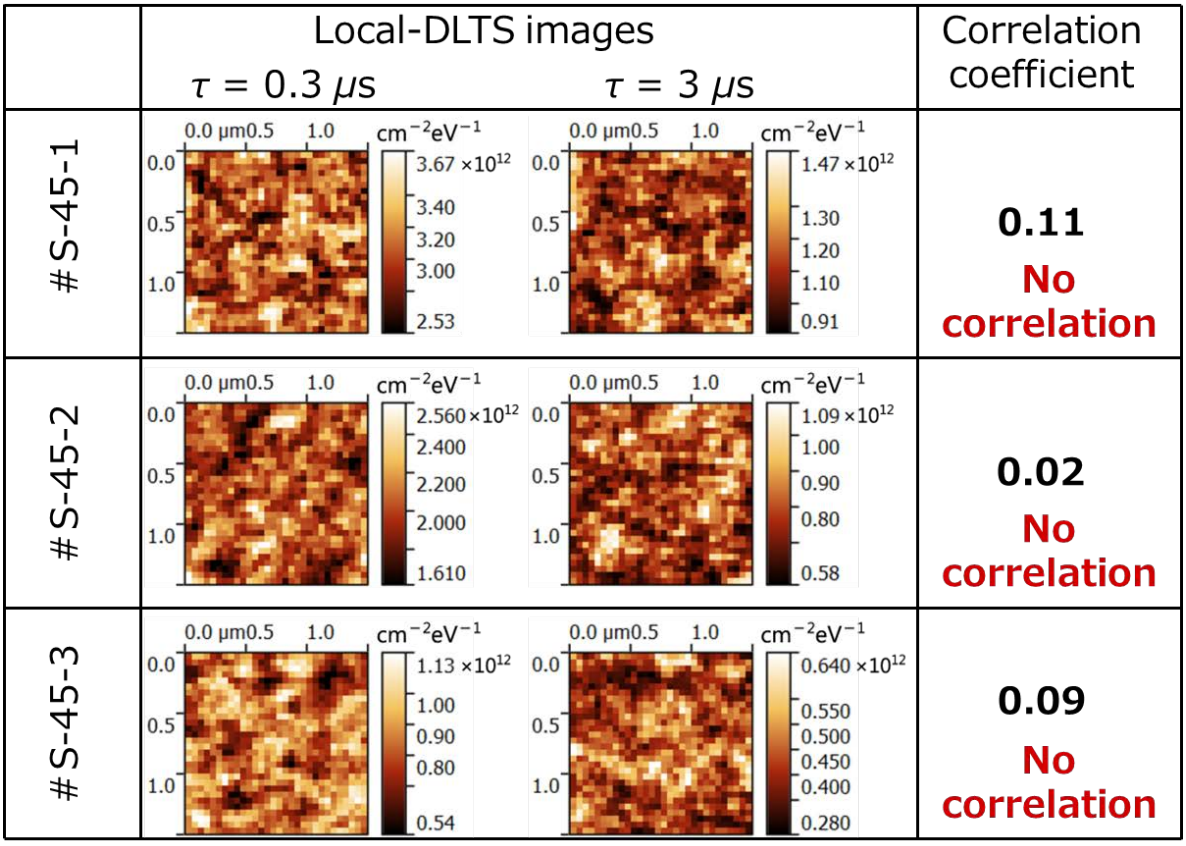

Figure 3. Quantitative imaging of interfce trap density D_{it} converted from local-DLTS signals for the tome constants τ = 0.3 μs and 3 μs. Assuming capture cross-section as 10^{-16} cm^2, the time constants 0.3 μs and 3 μs correspond to energy depth of 0.24 eV and 0.30 eV below the conduction band, respectively. The averaged D_{it} are same order of magnitude as D_{it} values at corresponding energy level measured by macroscopic High-Low method. All images have dark and bright areas with feature size of a few 100 nm. In addition, the images with different time constant showed different distribution, which implies that the distribution of interface traps depends on time constant, or suggests the physical origin of interface trap with different energy level is different.