PCSI

Room Keauhou II - Session PCSI-TuE

Rump Session: 2D or not 2D?

Moderator: Jun Zhu, Penn State University

7:30pm **PCSI-TuE-1 III-V Transistors for nm Logic and 100-1000 GHz Wireless*, Mark Rodwell,*** University of California, Santa Barabara **INVITED**

We examine the opportunities for nm III-V electron devices both in VLSI logic and in mm-wave (and sub-mm-wave) wireless communications.

Tunnel FETs (TFETs) are being developed for high on-off current ratios at low operating voltages, enabling low-power VLSI. III-V heterojunction TFETs offer direct (vs. phonon-assisted) tunneling, low tunnel barrier energy, and low electron effective mass. TFET on-currents are nevertheless very low; consequently TFET logic will be very slow. We are developing modified (triple-heterojunction) TFETs [1]. In these, added wide-bandgap source and channel layers increase the junction built-in potential, increasing the junction field and thereby decreasing the tunneling distance. Confinement with transport decreases the hole mass. The tunneling probability is greatly increased, proportionally increasing the on-current and logic speed. As the heterojunctions must be perpendicular to the semiconductor-dielectric interface, both convention TFETs are profoundly difficult to fabricate. Addressing this, our fabrication process, which we are developing, uses template assisted selective epitaxy [2].

Wireless communications will soon move to 5G (28, 38, 57-71, 71-86GHz); research now explores 100-1000 GHz systems. Above ~200GHz, CMOS provides little or no amplification, and scaling below ~32nm does not improve this. We must develop transistors for the low-noise and high-power stages in 100-200GHz systems, and for all stages at higher frequencies. InP HBTs, useful for power, have reached 1.1THz f_{max}. To further improve bandwidth, we are exploring TESA processes to form devices with buried dielectric layers in the base-collector junction. The base contact can be made wider for reduced resistance while the buried dielectric layer maintains low junction capacitance. InP HEMTs, useful for noise, have reached 1.5THz f_{max}. To further improve bandwidth, we are developing nm InAs MOS-HEMTs, with ALD ZrO_2 gate dielectrics, 5nm channels, and modulation-doped access regions surrounding the gate.

[1] P. Long, *et al*., 2017 Device Research Conference, June, Notre Dame.

[2] L. Czornomaz, *et al*., 2015 VLSI Symposium, June, Kyoto, Japan

8:00pm **PCSI-TuE-7 Emerging Frontiers of 2D Materials: From Low-Energy and Bendable Electronics to Quantum-, Spin-, and Valley-Enabled Devices*, Roland Kawakami,*** The Ohio State University **INVITED**

2D materials research began with graphene, but has expanded far beyond to include transition metal dichalcogenide (TMD) semiconductors, hexagonal boron-nitride (h-BN) insulators, and other 2D van der Waals systems. Most notably, the 2D materials can be stacked into vertical heterostructures, where proximity effects and transport driven processes can create properties that are not present in the individual 2D sheets. In this talk, I will review some of the exciting trends in 2D materials research as it relates to electronic and photonic devices. Some of the more near term research involves develop novel devices such as tunneling field effect transistors for low energy electronics, as well as printable inks for large area and bendable electronics. Looking further into the future for 2D materials, there are new opportunities for spin-based logic, valley-polarized electronics and photonics, and single photon emitters for quantum information. The advent of spin field effect switches in graphene/TMD heterostructures, monolayer ferromagnets, long valley lifetimes of holes and indirect excitons, and robust single photon emission from defects in h-BN are among the recent new discoveries that fuel the excitement for 2D materials research and their potential applications.

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