Li-ion Synaptic Transistor for Low Power Analogue Computing (LISTA)

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Neuromorphic networks that emulate brain plasticity and adaptive learning will revolutionize artificial intelligence and computing. The key element for neuromorphic networks is the artificial synapse, which emulates the function of its biological counterpart using strictly solid-state components. Necessary attributes of an artificial synapse are non-volatile memory and history-dependent analogue states. These synapse characteristics can be realized using two-terminal memristive devices. However, two-terminal memristors cannot readily utilize existing computational algorithms designed for CMOS circuits, thus requiring development of new algorithms. Recently, three-terminal, transistor-like memristive devices utilizing an ionic liquid gate to control source-drain resistance by injection or extraction of oxygen vacancies have been demonstrated at Harvard and IBM. This functionality enables the implementation of spike time dependent plasticity (STDP) by converting the time difference between source (pre-neuron) and drain (post-neuron) spikes into a gate voltage. The exact channel conductance state achieved through a set of voltage pulses determines the synapse weight. The Harvard and IBM approach, however, has two principal drawbacks: 1) it requires a liquid gate to effectively inject or withdraw oxygen vacancies 2) switching is slow (~seconds) even at 160 ^{o}C due to the sluggish motion of oxygen ions in solid lattices at or near room temperature. To address these shortcomings, we describe an alternative synaptic transistor based on insertion/extraction of Li-ions from a Li_xCoO_2 channel. Similarly to oxygen vacancies, Li-ions act as dopants, contributing a mobile electron or hole every Li-ion insertion or extraction, depending on the specific material. Compared to O-vacancies, however, Li-ions move as interstitials with much lower activation energy. Since Li diffusivity at room temperature is relatively high, the ionic liquid gate is replaced in our device by a solid Li electrolyte to realize all-solid state synaptic transistors.

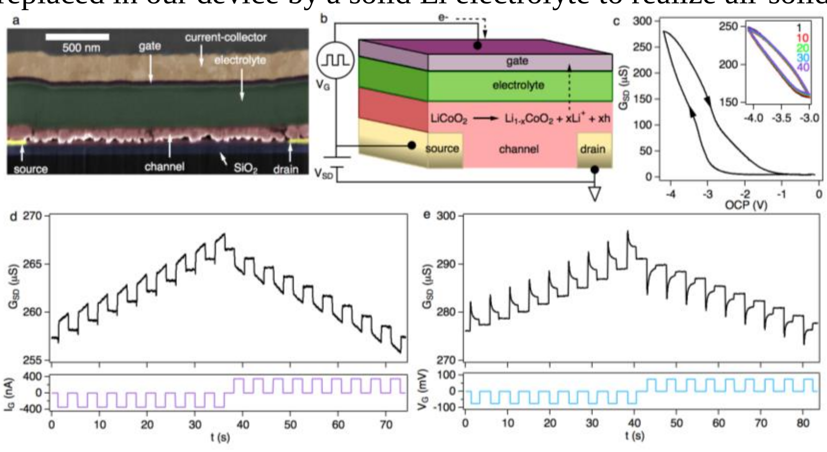

Figure 1. Structure and operation of a LISTA device. **a,** False color SEM micrograph in cross section. **b,** Schematic of device with $Li_{1-x}CoO_2$ channel material. **c,** source-drain conductance G_{SD} as a function of gate voltage, with source-drain bias of 100 mV. The inset shows repeated cycling over the voltage window -4.1 < *OCP* < -3.0. The cycle numbers 1, 10, 20, 30 and 40 are shown in various colors. **d,** Plot of the device conductance $G_{SD}(t)$ during current pulsing and **e**, voltage pulsing to the gate electrode.