## MBE
## Room Silver Creek - Session MBE-2MoM

### Heterogeneous Integration
**Moderator:** Zbigniew Roman Wasilewski, University of Waterloo

10:30am **MBE-2MoM11 MBE Growth of High-Quality GaAs on C-plane Sapphire Substrate**, ***Samir Kumar Saha***, *R. Kumar, A. Kuchuk, Y. Maidaniuk, Y. Mazur, S.Q. Yu, G. Salamo,* University of Arkansas

Heteroepitaxy of III-V semiconductor is a well-established field. Generally, the term heteroepitaxy is used to denote the growth of dissimilar materials having similar crystal structure but different lattice constant. Very few examples exist in literature regarding single-crystal epitaxy of two semiconductors with dissimilar crystal structures such as cubic on wurtzite or cubic on trigonal. There have been a few works regarding cubic SiGe growth on a trigonal sapphire substrate. In this report, we discuss the growth of quality GaAs buffer on c-plane sapphire. Our motivation to grow GaAs on sapphire is based on its potential use in III-V microwave photonics, optoelectronics and electronics owing to the properties, such as, a large contrast in refractive index between GaAs and sapphire, the high resistivity of sapphire substrate and the transparency of the sapphire substrate near the III-As band gap.

When grown on c-plane sapphire, GaAs tend to grow along the [111] orientation. In our experiments we have observed that the growth of GaAs on sapphire has a small range of parameter for best quality material. In this window, our samples show a surface RMS roughness as low as 1.6 nm; a rocking curve linewidth comparable to the GaAs substrate at 90 arcsec, good photoluminescence efficiency, and suppression of twinning in GaAs to less 0.1%. The latter was accomplished by utilizing different growth strategies, such as, a low temperature initial layer, multiple annealing cycles and by optimizing growth parameters (growth temperature and arsenic flux).

10:45am **MBE-2MoM12 Controlling Nucleation and Growth of IV-VI Rocksalt PbSe and PbSnSe on III-V Zincblende Substrates**, ***Brian Haidet***, *E. Hughes, K. Mukherjee,* University of California, Santa Barbara

Pb-rich PbSnSe is a rocksalt semiconductor with a conventional direct bandgap ranging from 0.3 eV to 0 eV, after which for alloy compositions >30% Sn, PbSnSe becomes a topological crystalline insulator with an inverted gap[1]. Recognizing that both infrared and potential quantum technologies require very high material quality, to us this system provides a fantastic opportunity to study heavily mismatched cross-materials-system heteroepitaxy. Previously, IV-VI growth has been dependent on fluorite substrates and buffer layers[1,2], but in this work, we explore PbSe growth on more conventional III-V substrates. This IV-VI/III-V interface incorporates a change in valency, surface charge, and crystal structure. GaSb and InAs are both nearly-lattice-matched to PbSe, but present chemically different surfaces, making this a model system for investigation.

We demonstrate that the nucleation behavior of PbSe can be controlled by modifying the III-V surface reconstruction and chemistry prior to growth. Specifically, by exposing arsenide surfaces to PbSe flux at high temperature, we can convert the surface into a suitable template for single-orientation nucleation of PbSe, resulting in a cube-on-cube epitaxial arrangement for both (001)- and (111)-oriented substrates. Interestingly, this result does not extend to antimonide surfaces or untreated arsenide surfaces, where the interfacial energy between substrate and film is so high as to make PbSe nucleation orientationally ambivalent. Uncontrolled nucleation results in a mixture of (001), (110), and {221}-type grains on (001) substrates, and rotations of (111) grains on (111) substrates. This behavior highlights the importance of surface chemistry in this heteroepitaxial system.

With this method, we have produced (001)-oriented PbSe films with 369 and 185 arcseconds of tilt about the [110] and [1-10] directions, respectively, in films only 80 nm thick. This result is on par with multi-micron-thick films from other studies[3]. The ability to recover higher-quality material in thinner layers has great implications for devices, especially those with electrically active heterojunctions. On (111)-oriented substrates, we further demonstrate for the first time growth of rocksalt compositionally (metamorphic) graded buffers in the PbSnSe alloy system, opening new avenues for fabrication of IV-VI devices.

[1] G. Springholz, G. Bauer. Semiconductors, IV-VI, in: Wiley Encycl. Electr. Elec. Eng. (2014)

[2] P. Müller, A. Fach, J. John, A. N. Tiwari, H. Zogg, and G. Kostorz. J. Appl. Phys. 79 (1996)

[3] X.J. Wang, Y.B. Hou, Y. Chang, C.R. Becker, R.F. Klie, T.W. Kang, R. Sporken, and S. Sivananthan. J. Cryst. Growth 311 (2009)

11:00am **MBE-2MoM13 On the Origin of Hillock Formation during the Growth of InGaAs/InAlAs Superlattice on InP(111) Substrates**, ***Ida Sadeghi***, University of Waterloo, Canada; *A. Pofelski, G.B. Botton,* McMaster University, Canada; *Z.R. Wasilewski,* University of Waterloo, Canada

InAlAs/InGaAs growth on polar InP(111) wafers offers physical properties of interest for optoelectronic devices. For instance, strain-induced internal piezoelectric field in the [111] orientated heterostructures can be useful for applications operating at the 1.55 µm wavelength [1]. However, growth on (111) substrates is much less understood than that on the conventional (001) substrates. Strong surface roughening with high density of hillocks and pits is the primary challenge for growth on (111) substrates.

Previous studies mainly focused on the surface morphology of the structures grown in [111] direction with less attention on the underpinning of the hillock formation [2]. In this study, scanning transmission electron microscopy (STEM) was used to elucidate the origin of the hillocks and surface roughening on singular and vicinal (111) surfaces. STEM analysis showed that the hillocks on singular (111) surfaces are formed due to the underlying stacking faults and twins. Observed strong suppression of twins and consequently hillocks on vicinal (111) surfaces (Fig. 1) is believed to result from minimizing (111) island formation through step flow promotion, as discussed in Ref. [3]. Since stacking faults and twins are caused by the local insertion of one monolayer of wurtzite (W) phase between two zinc blende (ZB) phases, suppression of phase instability between ZB and W structures is the most important challenge to overcome. Compared to the near lattice-matched growth of AlGaAs on GaAs(111) substrates [4], the difficulty is further compounded for (In,Al,Ga)As growth on InP(111) substrates due to the large bond length differences between InAs, AlAs, GaAs and InP.

[1] E.A. Caridi et al., Appl. Phys. Lett. **56**659 (1990).

[2] C.D. Yerino et al., *J. Vac. Sci. Technol. B*, 35 010801 (2017).

[3] I. Sadeghi et al., *J.Vac.Sci.Technol. B*37 031210 (2019).

[4] Y. Park et al., *J. Vac. Sci. Technol. B***18**1566 (2000).

11:15am **MBE-2MoM14 Effectiveness of $In_{0.1}Ga_{0.9}As$ Dislocation Filters to Reduce Threading Dislocation Density**, ***Chen Shang***, *J. Norman, A. Gossard, J. Bowers,* University of California, Santa Barbara

Epitaxially grown semiconductor laser material on Si (001) with quantum dot (QD) active regions is important for lower cost optical interconnects. The projected QD laser lifetime is more than a million hours at 35 °C under continuous-wave (CW) operation [1]. The drastic reliability improvement is primarily due to the reduction of threading dislocation density (TDD) on the GaAs on Si buffer surface. Further reduction of TDD is needed for high temperature reliability and future integration with Si waveguides. Here, we investigate the effectiveness of $In_{0.1}Ga_{0.9}As$ dislocation filter layers grown on GaAs with different TDD. We investigate the filtering mechanism and provide insights to further lowering of TDD while also reducing total epitaxial thickness.

To generate GaAs surfaces with different TDD, a GaAs buffer layer (Fig. 1a) was grown on low defect density GaP on Si templates from $NAsP_{III/V}$, GmbH. Temperature cyclic annealing (TCA) was then performed with temperature ranging from 400 °C to either 700 °C or 735 °C, and 4, 8, or 12 cycles. The surface roughness of all 6 samples are similar, according to atomic force microscopy (AFM) measurements. 200 nm $In_{0.1}Ga_{0.9}As$ and 300 nm GaAs were then grown after TCA at 500 °C (Fig.1a). TDD was measured with electron channeling contrast imaging (ECCI) both before and after the growth of the filter layer. The results are summarized in Fig.1(c). Higher number of cycles reduced TDD with the effect being more prominent at lower maximum cycling temperature. The TDD is further reduced after the growth of the $In_{0.1}Ga_{0.9}As$ filter layer. The effectiveness of the filters, namely the percentage TDD reduction, on different TDD is shown in the inset of Fig.1(c). Although samples with maximum temperature of 700 °C have higher starting TDD, the filtering effectiveness is lower than the samples with maximum temperature of 735 °C. This implies that the filtering is facilitated not only by lateral motion of existing TDs, but also the formation of new glissile TDs as bridges between the existing TDs. The effect of initial GaAs thickness, filter layer structure, and relaxation asymmetry on the filtering effectiveness will be discussed.

11:30am **MBE-2MoM15 Study of Pit Formation in MBE Grown GaP on Misoriented Si Wafers**, ***Srinath Murali***, *C. Zhang, R. King, C. Honsberg,* Arizona State University

Heteroepitaxial growth of III-V materials such as GaAs, InGaP, GaAsP on Si have been a subject of keen interest for several years due to its potential for high performance optoelectronic devices. However, the inherent difference in lattice constants between these compounds and silicon lead to the formation of large number of crystalline defects [1]. Additionally, the growth of polar films on non-polar substrates gives rise to the formation of antiphase domains at the interface that propagate throughout the film [2]. Some of these defects can be suppressed by the growth of a GaP buffer layer before growing the target structure, making GaP a key part of III-V integration with silicon [3]. The surface quality of GaP films will determine the quality of subsequent III-V layers grown and impact the electrical properties of these material systems.

In this work, the focus is on demonstration of epitaxially grown GaP on misoriented Si wafers using Molecular Beam Epitaxy. The GaP layer acts as a buffer between the Si substrate and a Dilute Nitride-GaNP material. The epitaxial GaP layers were grown on Si substrates of precise (001), 4° offcut in (110) and 6° offcut in (110) orientations by a combination of Migration Enhanced Epitaxy (MEE) and MBE methodologies. The reflection high energy electron diffraction (RHEED) patterns observed (fig. 1a) were a mixture of spots and streaks, indicating the presence of some islands in conjunction flat layers. Atomic force microscopy (AFM) imaging suggests the presence of pits on the GaP surface (fig. 1b and 1c). These pits could be a result of melt back etching on the Si substrate caused by the Ga adatoms impinging on the substrate during growth process. Pit formation due to melt back etching will be verified by removal of grown GaP layer and characterizing the Si substrate surface by further AFM imaging. The effect of substrate orientation and the growth technique on the pit formation along with methods to suppress them will be presented.

11:45am **MBE-2MoM16 GaSb-Based Mid-Infrared Photonic Devices Monolithically Integrated onto Silicon**, ***Peter Carrington***, Lancaster University, UK

GaSb-based materials can be used to produce high performance photonic devices operating in the technologically important mid-infrared (MIR) spectral range (2 to 5 µm). Direct epitaxial growth of GaSb on silicon (Si) is an attractive method to reduce manufacturing costs and opens the possibility of new applications in lab-on-chip MIR photonic integrated circuits. However, the fundamental material dissimilarities including the large lattice mismatch, the polar-nonpolar character of the III-V/Si interface and differences in thermal expansion coefficient lead to the formation of threading dislocations (TDs) and antiphase domains (APDs) which effect the device performance. This work reports on the molecular beam epitaxial (MBE) growth of high quality GaSb-based materials and devices onto Si. This was achieved using a novel growth procedure consisting of; an efficient AlSb interfacial misfit array, a two-step GaSb growth temperature procedure and dislocation filters, resulting in a low defect density, anti-phase domain free GaSb buffer layer on Si. A nBn barrier photodetector based on a type-II InAs/InAsSb superlattice was grown on top of the buffer layer. The device exhibited an extended 50 % cut-off wavelength at 5.40 µm at 200 K which moved to 5.9 µm at 300 K. A specific detectivity of 1.5 $x10^{10}$ Jones was measured corresponding in an external quantum efficiency of 25.6 % at 200 K. InAsSb p-i-n LEDs were also grown on the GaSb-on-Si buffer layer which showed bright room temperature electroluminescence (EL) peaking around 4.5 µm.

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