Advancing Piezo-Gated Transistor Performance by Bilayer of V-doped ZnO and Mesoporous PVDF-TrFE.

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Abstract:

In recent years, technology has rapidly advanced, enabling the development of flexible wearable electronics with great potential for applications such as nanogenerators and pressure sensors. Among flexible materials, β-phase PVDF-TrFE, which exhibits piezoelectric properties (d_{33}=30–40pC/N), stands out as a promising composite. This polymer has a semicrystalline structure and displays excellent piezoelectric and ferroelectric properties while maintaining flexibility. However, VZO (d_{33}=12–22pC/N) is also a piezoelectric material, and we aim to improve the device output by depositing it on PVDF-TrFE.

In this study, we aimed to enhance the flexibility and piezoelectric performance of PVDF-TrFE by blending it with zinc oxide nanoparticles and subjecting the mixture to thermal annealing at 120°C. We then applied 11,000 V through corona poling to align the dipole directions within the composite, followed by etching the ZnO to create a porous structure. Additionally, we used radio frequency magnetron co-sputtering that uses ZnO and V_2O_5 as targets to deposit VZO thin film on both sides of the PVDF-TrFE to serve as conduction pathways. Finally, we deposited two Au electrodes to make a piezoelectric gate transistor device.

In the XRD analysis, we examined unpoled and corona-poled samples. The XRD patterns of the unpoled sample showed two peaks corresponding to the α phase which has negatively affects the piezoelectric properties. After poling, the pattern of the poled sample confirmed that the β phase completely dominates the PVDF-TrFE.

We investigated the current output of the piezoelectric gate transistor under various mechanical stresses at a 1V bias and 1Hz frequency. Devices with different dipole orientations exhibited opposite behaviors. Applying mechanical stress to the positively polarized surface generated negative charges at the VZO and PVDF-TrFE interface, creating a depletion region in the top surface channel and reducing current. Conversely, this led to an accumulation region, enhancing current. By applying a piezoelectric field to the gate, we could adjust the semiconductor channel's resistance and control current flow. This technique significantly advances the piezoelectric gate transistor device, paving the way for advanced applications in flexible and wearable electronics and sensing technologies.

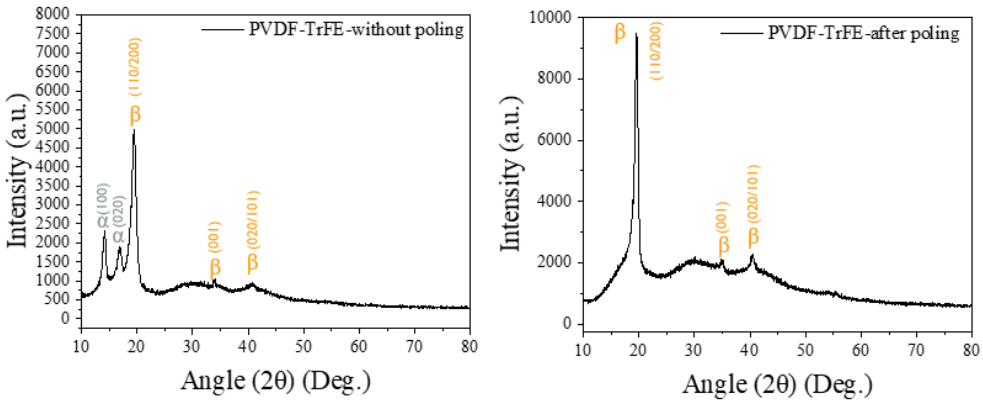

Fig. 1. XRD patterns of PVDF-trFE (a) without poling and (b) after poling

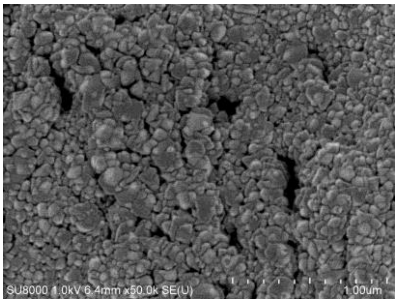

Fig. 2. Plan-view image of VZO on Mesoporous PVDF-TrFE

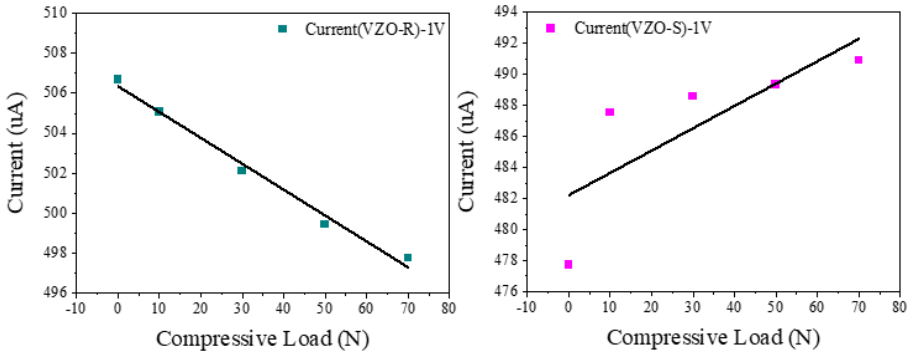

Fig. 3. Current-Load plots of the two devices with different dipole orientations

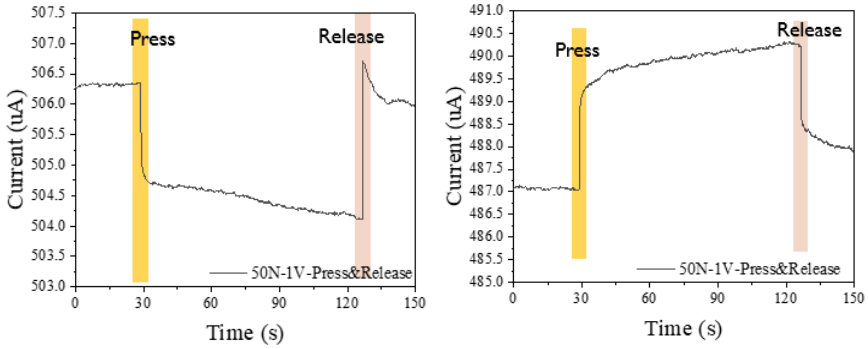

Fig. 4. Current-Time plots of the device with (a) depletion region (b) accumulation region