Plasma and Vapor Deposition Processes
Room Palm 3-4 - Session PP3-WeA

ALD, CVD Coating Technologies

Moderators: Hiroki Kondo, Kyushu University, Japan, **Frederic Mercier**, University of Grenoble Alpes, France

2:00pm **PP3-WeA-1 Electrical Conductivity as a New Parameter for SAMs-Free Area-Selective Atomic Layer Deposition, from Principles to Photoconversion Devices**, ***David Horwat***, Institut Jean Lamour/Université de Lorraine, France **INVITED**

Area-selective atomic layer deposition (AS-ALD) has gained a lot of attention in recent years due to the possibility of achieving accurate patterns in nanoscales features, especially for complex 2D or 3D nanostructures [1], which makes this technique compatible with the continuous downscaling in electronics devices. AS-ALD is usually achieved by deactivation of part of the surface by self-assembly monolayer (SAMs) of certain molecules [2]. Here we propose a different approach that consists in modulating a property of the substrate to achieve localized growth of different materials, its electrical conductivity. This concept is demonstrated by selective growth of high quality metallic Cu, and semiconducting Cu_2O or absence of deposition, depending on the value of the electrical conductivity and substrate temperature. We will present our understanding of the process and will highlight some of its potentials. It is for instance possible to interface n and p semiconductors or semiconductors and metals with local control in order to fabricate demonstrator devices [3-5] of potential interest for photoconversion purposes.

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3. C. de Melo et al. ACS Applied Materials and Interfaces 10 (2018) 37671-37678

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2:40pm **PP3-WeA-3 Direct ALD Deposition by µDALP™. Precision Coatings for Next Gen Devices**, ***Mira Baraket***, ATLANT 3D Nanosystems, Denmark

Advancements in the microelectronics sector demand the ability to create high-quality films with nanoscale accuracy to pattern complex features on substrates. Area-selective deposition (ASD) meets this demand by enabling the selective formation of films on specific surface regions while preventing deposition elsewhere[1]. Atomic Layer Deposition (ALD), a well-established technique in the semiconductor field has been widely investigated for ASD applications. However, this method often requires initial surface treatments, surface functionalization, or alterations to the process[2].

ATLANT 3D has introduced an innovative technology named microreactor Direct Atomic Layer Processing - µDALP™, enabling precise localized thin film deposition with accuracy down to a few hundred microns, incorporating all conventional ALD advantages (Fig. 1 (a)). This technology leverages a specialized design of micronozzles to spatially separate precursors and reactants, facilitating rapid film deposition at atmospheric conditions (Fig. 1(b))[3]. The µDALP™ technology stands out for its vertical atomic monolayer precision, achieving an accuracy of 0.2 nm. It is especially effective for selective patterning across diverse surfaces, including microfluidic channels, optical gratings, and nanostructured interfaces, showcasing its versatility and precision. Moreover, this technology enables fast and cost-effective prototyping of devices, facilitating a level of design creativity and optimization that is challenging by traditional thin film deposition approaches.

ATLANT 3D's technology has been successfully utilized to innovate in fields such as optics and photonics, quantum devices, microelectromechanical systems (MEMS), RF electronics, cutting-edge memory technologies, advanced packaging, and energy storage, showcasing its wide-ranging application potential. In this talk we will explain the significant contributions of our µDALP™ technology to the evolution and expansion of thin-film manufacturing and discuss the wide array of opportunities it presents across different sectors.

Fig. 1. (a)Top view of aligned Si trenches (aligned horizontally) coated with a perpendicular line of TiO_2 (low magnification SEM). (b) Microfluidic precursor delivery concept: Schematic view of the delivery nozzle in frontal view (top) and in cross-section (lower panel).

References

(1)Parsons, G. N.; Clark, R. D., **2020**, *32* (12), 4920–4953.

(2)Mackus, A. J. M.; Merkx, M. J. M.; Kessels, W. M. M., *Chemistry of Materials* **2018**, *31* (1), 2–12.

(3)Kundrata, I.; Barr, M. K. S.; Tymek, S.; Döhler, D.; Hudec, B.; Brüner, P.; Vanko, G.; Precner, M.; Yokosawa, T.; Spiecker, E., *Small Methods* **2022**, *6* (5), 2101546.

3:00pm **PP3-WeA-4 Selective Generation of Nanoparticles in Plasma-Enhanced CVD and Deposition of Carbon Films with Low Compressive Stress**, ***Kazunori Koga***, Kyushu University, Japan **INVITED**

The stress of diamond-like carbon (DLC) films has been a significant issue in enhancing the performance of protective coatings used in dry etching masks, automotive parts, and battery electrodes. Traditionally, metal nanoparticles have been incorporated into the films to reduce stress. However, this approach often leads to metal contamination, which deteriorates the performance of semiconductor devices. In this study, inspired by the incorporation of metal nanoparticles, we aimed to alleviate stress by incorporating carbon nanoparticles (CNPs) into DLC films. As a first step, we successfully controlled the size of the nanoparticles using plasma chemical vapor deposition (CVD). Subsequently, we managed to control the amount of CNPs deposited on substrates using capacitively coupled plasma CVD, a technique widely employed for large-area deposition. Transmission electron microscopy (TEM) images revealed that the deposited CNPs could be classified into two size groups: the smaller group with a mean size of approximately 2.9 nm, and the larger group with a mean size of around 16 nm. We successfully controlled the amount of CNPs on the films with discharge duration. We shortened the discharge time to prevent the nanoparticles from piling up on the substrate, resulting in sparse deposition on the film surface. The amount of nanoparticles deposited was expressed as a percentage of nanoparticles per unit area of the film, defined as the coverage (Cp) of CNPs. Based on these results, we fabricated a-C:H/CNP/a-C:H sandwich-like films using the plasma CVD. A mixture of Ar and CH_4 gases was introduced from the top of the chamber at flow rates of 19 sccm and 2.6 sccm, respectively, maintaining a total pressure of 0.3 Torr. These conditions were consistent with those used for CNP deposition. The mass density of the deposited a-C:H films was 1.88 g/cm^3. We observed that the film stress decreased with increasing Cp, from 1.59 GPa at Cp = 0% to 1.02 GPa at Cp = 8.9%, with a similar value at Cp = 15.9%. This represents a reduction rate of 35.8%. These results indicate that incorporating a small amount of CNPs can effectively reduce film stress. Moreover, we successfully expressed the stress reduction rate in terms of Cp using experimental results for different sandwich film thicknesses.

3:40pm **PP3-WeA-6 Temperature Influence on the Chemical Vapor Deposition of Nitrogen-Doped SiC Polycrystalline Films for Brain-Implantable Devices**, *Michalis Gavalas,* SIMaP, CNRS, University Grenoble Alpes, France*; Konstantinos Zekentes,* Microelectronics Group/IESL-FORTH, University of Crete, Hellas, Greece*;* ***Frederic Mercier,*** SIMaP, CNRS, University Grenoble Alpes, France

Silicon carbide (SiC) is a wide-gap semiconductor, with high chemical stability, that is proposed as a functional material for biomedical applications [1,2]. Epitaxial and polycrystalline SiC has been proposed for neural recording and stimulation electrode devices [3,4]. Unlike the epitaxial case, polycrystalline 3C-SiC is advantageous as it can grow on various substrates (silicon, silica, diamond, sapphire etc) and at lower temperatures. However, the state of the art for the polycrystalline SiC based neural interfaces is still poor. Dense layers of poly-SiC with low resistivity and low stress combined with the good chemical stability of SiC are required for the fabrication of neural interfaces [3,4]. Towards this aim, polycrystalline nitrogen doped 3C-SiC thin films, are grown on 2 inches Si wafers by low-pressure chemical vapor deposition (LPCVD) technique with the aim to be used as support and active material in microelectronic devices and for neural interfaces. The effect of deposition temperature on the structural, mechanical and electrical properties is investigated. Growth rate is varying from 1 µm/h to 14 µm/h, along with the deposition temperature. We show that we can control simultaneously the structural and electrical properties of polycrystalline SiC by changing the deposition temperature. Films with resistivity as low as (10.0 ± 0.5) mΩ·cm, low residual stress of (245 ± 13) MPa and RMS surface roughness of (159 ± 54) nm are achieved. Furthermore, the chemical stability of SiC in physiological fluids is investigated and we show that polycrystalline SiC can be a suitable

material for neural interfaces applications.

[1] Maboudian, R. et al., J. Vac. Sci. Tech., 31, 5, 2013
[2] Saddow, S. et al., Microm., 13(346), 1-21, 2022
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