Functional Thin Films and Surfaces
Room Pacific F-G - Session C2-2-FrM

Thin Films for Electronic Devices II

Moderators: Dr. Julien Keraudy, Oerlikon Balzers, Oerlikon Surface Solution AG, Liechtenstein, **Dr. Jörg Patscheider**, Evatec AG, Switzerland

8:00am **C2-2-FrM-1 3D Device Integration Technology for AI Computing***, S. Chang,* Powerchip Semiconductor Manufacturing Corporation, Taiwan*;* ***Chun-Lin Lu,*** Powerchip Semiconductor Manufacturing Corporation, USA **INVITED**

To cope with the massive computation requirement of semiconductor chips in 5G and AI, 3D device integration incorporating with new system architectures is developed, to mitigate the computational von Neumann memory wall via minimized data movement. Both the 3D Memory-Logic chip stacking and monolithic SoC integration are developed for near-memory and in-memory analog computing, to perform high bandwidth and efficient power performance, leading AI computing toward a green technology era.

3D Memory-Logic Chip Stacking

We focus on wafer-on-wafer Memory-Logic 3D stack technologies, including (1). Oxide bond with paired TSV (Through Silicon Via), (2). Hybrid bond with TSV middle embedded in DRAM, and (3). Multi-DRAMs stack on Logic. The interconnect density is among 1E4-1E6/mm^2 range.

For intensive data-movement computation applications, hybrid bond with 2-3μm Cu bond pitch is developed to provide 1E6/mm^2 high interconnect density and < 0.5Ω low interconnect (Via-pad-bond-pad-Via) resistance. After implementing dispersive DRAM I/O and skipping interface PHY circuit in the system design, 55nm-node Logic chip and 38nm-node customized 6GB DRAM chip are bonded together to demonstrate 3-9X excellence in system performance, better than the products using advanced Logic chip while choosing commercial DRAM with standard I/O interface.

For AI image recognition applications, oxide bond with paired TSV is implemented for Logic-DRAM stacking, which a 10μm/15μm dual TSV with 20μm pitch is used for interconnection, providing < 0.2Ω (pad-TSV-Cu line-TSV-pad) resistance and 1E4/mm^2 interconnect density. The AI inference (# of image recognition/s) performance is expected to improve > 50%, as the I/O bandwidth enlarges 8X to 51.2GB/s. These 3D schemes can minimize energy consumption to <1pJ/bit during data movement.

3D Monolithic SoC for Analog in-Memory Computing (AiMC)

AiMC eliminates data movement during computation, offering low-power multiply-accumulate (MAC) operations in AI computing. To improve the poor power consumption and worse temperature variation reported in some emerging memory AiMC, monolithic 3D Si/CAAC (c-axis-aligned crystalline)-IGZO 3T1C AiMC chips with ultra-low operation cell currents (<1 nA/cell), multiple analog states (8 and 64), and high computing efficiency (143-210 TOPS/W) are demonstrated [1,2]. We further implement Ferroelectric material into the MIM capacitor to keep the MNIST inference accuracy > 90% even at 125^{o}C high temperature operation, while retention time > 50hrs. We believe it is a good candidate for the next-gen AI computing.

Ref. [1,2] IEDM 2021/2022

8:40am **C2-2-FrM-3 Magnetic Nanolaminates Deposited by Magnetron Sputtering for Next Generation Electronic Devices***, **Claudiu V. Falub**, M. Bless, J. Richter, X. Zhao, H. Rohrmann, M. Tschirky, M. Padrun,* Evatec AG, Switzerland

The emerging Internet-of-Things (IoT) and artificial intelligence (AI) applications, combined with the ongoing miniaturization of mobile devices, has led to an increasing demand for heterogeneous systems that need to be integrated with the silicon complementary metal-oxide-semiconductor (Si-CMOS) platform, such as smart power management units based on integrated voltage regulators (IVR) and ultrahigh density non-volatile memory (NVM) cells. Besides numerous challenging surface engineering processes and corresponding equipment concepts for high volume manufacturing, the realization of these 3D monolithic architectures often requires advanced magnetic thin-film materials with precisely designed magnetic properties and thickness ranging from just a few tenths of nanometers up to several micrometers. In this talk we will illustrate some of these challenges using two examples where nanostructured magnetic thin film systems enable the requested functions for new generation electronic devices: (i) soft magnetic nanolaminates n×[m×(FeCoB/CoTaZr)/Al_2O_3] with tunable in-plane magnetic anisotropy that form the inductor cores for high-frequency RF filters and on-chip IVR; (ii) enhanced permeability dielectrics n×(FeCo/Al_2O_3) for single-layer Magnetoresistive Random Access Memory (MRAM) and programmable logic systems. These novel composite magnetic multilayers can be economically deposited on Si-CMOS wafers up to 300 mm in diameter using the high-throughput, multi-source, dynamic sputter systems in our portfolio, by simultaneously using two or more cathodes, and by carefully adjusting the thickness of individual nanolayers, i.e., by changing the cage rotation speed and sputter power of the individual stations [1]. Thus, due to the continuous rotation of the substrate cage, such that the substrates face different targets alternatively, the obtained thin films exhibited a nanolayered structure with very sharp interfaces in the case of soft magnetic nanolaminates [2], or a discontinuous structure with magnetic nanoparticles smaller than the superparamagnetic (SP) limit embedded in an insulating matrix [3]. We will discuss the interdependence of structure and magnetic properties in these thin films, and we will show how the latter can easily be tuned by choosing the sequence of magnetic and non-magnetic layers, and the thickness ratio of individual nanolayers.

[1] M. Bless, C.V. Falub, WO 2018/197305 A2.

[2] C.V. Falub et al., AIP Advances 8, 048002 (2018).

[3] C.V. Falub et al., AIP Advances 9, 035243 (2019).

9:00am **C2-2-FrM-4 Tungsten-Based Thin Film Metallic Glass as Diffusion Barrier between Copper and Silicon***, **Pei-Yu Chen**, J. You, C. Hsueh,* National Taiwan University, Taiwan

A qualified diffusion barrier layer in integrated circuits (IC) industry is essential to prevent the degradation of devices due to the rapid inter-diffusion of copper (Cu) and silicon (Si) for Cu metallization. In recent years, thin film metallic glass (TFMG) barrier materials are getting considerable attentions due to the advantages over the others by its thermal stability, low resistivity and excellent mechanical properties for some compositions. In this work, the performance of amorphous W–Ni–B TFMG as a diffusion barrier between silicon and copper layers is reported. The Cu (150 nm)/W–Ni–B (10 nm)/Si multilayered structures were fabricated by direct-current (DC) magnetron sputtering and annealing at 700–950 °C for 30 min in vacuum. The nanomechanical properties and thermal characteristics of the W–Ni–B TFMG was evaluated bynanoindentation and differential scanning calorimeter, respectively. The interfaces and microstructures of Cu/W–Ni–B/Si multilayered structures were characterized by a field-emission gun scanning electron microscope, X-ray diffractometer and transmission electron microscope. The findings indicated thatW–Ni–B TFMG showed extremely high hardness of 20 GPa and high reduced modulus of 217 GPa. In addition, W–Ni–B TFMG effectively blocked the intermixing of Cu and Si atoms at 800 °C. However, the failure ofW–Ni–B TFMG barrier against Cu and Si inter-diffusion was observed after annealing at 950 °C. Based on itsunique combinationof excellent barrier performance and high hardness, W–Ni–B TFMG could be regarded as a robust diffusion barrier for Cu interconnect technology.

9:20am **C2-2-FrM-5 Investigation of Properties and Microstructures of Ag-Cu Alloy Thin Films by Co-sputtering and First-principles Calculations**, ***Yu-Chieh Wang***, *C. Chen, F. Ouyang, H. Chen,* National Tsing Hua University, Taiwan

As the demands of electronic devices continue to be high performance and small transistor size, the current density in electronic devices will significantly increase and electromigration (EM) is expected to be a critical reliability issue. Thus, developing a high EM-resistant interconnect will be desired in the electronic industry. Ag interconnects have drawn many eyes because they possess extreme thermal and electrical conductivity. In addition, Ag has low stacking fault energy (SFE), which is easy to form a twinned structure that exhibits unique properties, including low electrical resistivity, high EM resistance, high mechanical properties, and high thermal stability. [1] Alloying is a common way to enhance the EM resistance, but it would simultaneously change SFE with the doping elements and concentration, further impacting the formation of nanotwin structure in thin films. In this study, we first investigated how the doping concentration of Cu affects SFE of Ag-Cu alloy thin films by first-principles calculations. Their intrinsic stacking fault energy (γ_{ISF}) and unstable stacking fault energy (γ_{USF}) were calculated. In addition, the wide-angle powder X-ray diffraction was conducted to measure the SFE of pure Cu and Ag-Cu alloys. Then, Ag-Cu alloy thin films with different doped Cu concentrations were fabricated by co-sputtering system and their properties and microstructures were studied. The results show all Ag-Cu alloy thin films exhibited highly (111) orientation. The results show that low Cu concentration in Ag films exhibits a higher density of nanotwin structure with good properties than pure Ag, demonstrating that adding Cu into Ag films can effectively lower stacking fault energy and facilitate the formation of nanotwin structure.

REFERENCES

[1] L. Lu, Y. Shen, X. Chen, L. Qian, K. Lu, Science 304 (2004) 422-426.

9:40am **C2-2-FrM-6 Multi-Step Method for the Fabrication of High-Performance Continuous Ultra-Thin Silver Films for Energy Applications**, ***Phillip Rumsby***, *B. Baloukas, O. Zabeida, L. Martinu,* Polytechnique Montréal, Canada

While Ag films offer significant advantages over other transparent conductors, their high surface energy gives rise to a Volmer-Weber, or island growth mode. In order to achieve films which are both thin enough to be highly transparent and continuous as so to ensure their conductivity, various methods are used to suppress the Volmer-Weber growth mechanism. Typically, one will decrease Ag adatom mobility via doping, lower Ag surface energy using nitrogen as a surfactant, or increase the surface energy of the substrate.

In this work we propose a novel method for producing continuous ultra-thin silver (Ag) films in different architectures and with different microstructural characteristics which exploits rather than avoids the high surface energy of Ag. Specifically, we deposit continuous films at an arbitrary thickness, and we then etch them using RF plasma until a desired thickness and performance are achieved. In this way, the surface energy minimization constraints which drive the agglomeration of adatoms into islands during film growth now help maintain the film morphology, as re-separation would increase the Ag surface area. Thus, continuous films can be produced at thicknesses below the threshold of continuous film formation during deposition.

The formation or breakdown of continuous Ag films can then be resolved using a facile *in-situ* ellipsometryapproach. After depositing a fully continuous Ag film onto a well-characterized substrate, the thickness and optical properties of the continuous Ag film are modeled. Then, using the obtained Ag optical properties and only the thickness of the layer is fitted, for each data acquisition. The mean square error (MSE) obtained on the fit then reflects divergence of the optical properties of the Ag layer from those previously modeled. Thus, as the film goes from continuous to discontinuous, plasmonic effects alter the optical properties and the MSE increases, and conversely for a discontinuous film achieving a continuous morphology during deposition, an example of which is shown in **Figure 1.**

We have validated the methods described above using *in-situ*-- sheet resistance measurements and cross-section transmission electron microscopy. Furthermore, we have demonstrated that this method enables the deposition of transparent, conductive, continuous thin films in atypical conditions, such as on a silica seed layer and at elevated temperatures, and can additionally be used to supplement the performance of Ag films in typical configurations. Finally, we propose additional processing steps between deposition and etching which may further improve coating performance.

10:00am **C2-2-FrM-7 Structural, Electrical, and Thermal Properties of Ge-Rich $Ge_2Sb_2Te_5$ Alloys**, ***Matias Kalaswad***, *A. Jarzembski, P. Kotula,* Sandia National Laboratories, USA*; T. Beechem,* Purdue University, USA*; M. King, D. Adams,* Sandia National Laboratories, USA

Materials which undergo vast and rapid transformations in optical, electrical, and thermal properties due to a phase change (e.g. amorphous to crystalline) at, or near, room temperature have long been utilized as key components in memory devices. Among these materials, germanium-antimony-telluride alloys, particularly $Ge_2Sb_2Te_5$ (GST), are especially prevalent due to their fast switching and large resistivity difference between the amorphous and crystalline states. Although chalcogenide phase change materials have been implemented in various non-volatile memories, efforts to improve phase stability and data retention in high-temperature (i.e. >100 C) environments (e.g. automotive) are still ongoing. Nearly a decade ago, a “golden composition” of a Ge-rich GST alloy exhibited a crystallization temperature of up to 250 C while still maintaining relatively fast (~80 ns) switching speed. Recent computational ab-initio studies have predicted that increasing Ge content in Ge-rich GST alloys leads to increased crystallization temperature, at the expense of phase stability in the form of segregation into regions of pure Ge and GST.

In this work, we present experimental results of structural, electrical, and thermal properties of three Ge-rich GST alloys: $Ge_2Sb_1Te_2$, $Ge_5Sb_2Te_4$, and $Ge_3Sb_1Te_2$. These are also compared to a benchmark GST film. From in-situ X-ray diffraction experiments, the Ge-rich GST alloys are observed to crystallize into cubic GST at temperatures between 250 C and 260 C, which is consistent with previous reports of similar alloys. Raman measurements generally support the XRD results, with cubic Sb-Te bonds forming around 200 C. Interestingly, Ge-Ge bonds form at 250 C, which is evidence of phase segregation as suggested by previous computational studies. In-situ measurements of the electrical resistivity show a decrease in resistivity beginning around 175 C for GST-212 and 230 C for GST-524 and GST-312, compared to 150 C for GST. The resistivity of all three Ge-rich GST alloys decrease by nearly four orders of magnitude, which is comparable to that of the benchmark GST alloy, albeit not as drastically (i.e. over a greater range of temperatures). Lastly, thermal conductivity measurements show an abrupt transition around 200 C from 0.2 W/mK to 0.7 W/mK for all three Ge-rich GST, which is nearly 50 C more than the transition temperature of GST.

10:20am **C2-2-FrM-8 Preparation and Electrical Properties of Tantalum Silicate Thin Films**, ***You-Sheng Lu***, *C. Chen, C. Huang, S. Chen, Y. Liu,* Ming Chi University of Technology, Taiwan*; W. Huang,* Chien Hwa Coating Technology Inc., Taiwan*; W. Yang,* General Research Institute for Nonferrous Metals, China

The electric resistivity and temperature coefficient of resistivity (TCR) of a material are important parameters when developing thin-film resistors for advanced electronics and electricity consumption. There are many materials that can be applied to thin film resistors, among which the tantalum silicate (Ta-Si-O) thin film material has attracted much attention, which is due to the excellent thermal stability and adjustable TCR of this material. However, the electrical properties of such thin film materials are highly correlated with the composition control and structure of the material. How to develop an efficient process method to more precisely control the composition and structure so as to obtain the required resistivity and TCR has always been an important issue. In the past, there were very few academic reports on the manufacturing process of these materials, so the related electrical research has been very limited. In this work, we prepared two targets with different target compositions, such as $Ta_{65}(SiO_2)_{35}$ and $Ta_{80}(SiO_2)_{20}$, to study the effects of target composition and sputtering power on the material structure and electrical behavior of the film. Our series of experimental results indicate that a Ta-Si-O film with a high Ta content can be produced by using a target material with a high Ta content, and a film with low resistivity and low TCR can be successfully produced with an appropriate sputtering power. According to material analysis, the excellent electrical properties of the film are highly related to the formation of Ta_5Si_3 as the main structural phase in the film.

10:40am **C2-2-FrM-9 Enhanced Reliability Characteristic Oftri-Gatepoly-Ge Charge Trapping Flash Memory with Ultra-Thin Tunneling Layer Engineering***, Che-Wei Lin,* National Tsing Hua University, Taiwan*; D. Ruan,* Fuzhou University, China*; K. Chang-Liao,* National Tsing Hua University, Taiwan

In this report, a high performance FinFET based junction-less charge trapping flash memory with poly-germanium (Poly-Ge) channel was successfully fabricated. Due to the high carrier mobility of Ge material, the operation speed of flash memory device can be improved by using a low temperature Poly-Ge channel. However, the reliability of poly-Ge flash device fabricated under harsh thermal budget limitation may be degradedafter inevitable thermal process. The reason may be Ge out-diffusion phenomenon and narrow energy band gap of Ge material. After stacking tunneling layer and plasma treatment, the memory device with aluminium oxynitride (AlON) tunneling layer may exhibit high programming speed, high erasing speed, long data retention time, and excellent endurance cycle. Firstly, those improvements can be attributed to better thermal stability and interface quality of AlON. Besides, the trap charge level of AlON might be much shallower than that of traditional silicon nitride trapping layer. It means that the operation speed can be further enhanced without scarifying data retention time and endurance cycle.

Author Index

Bold page numbers indicate presenter