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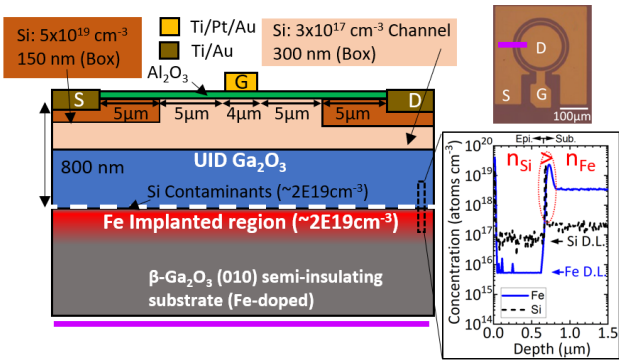

Fig. 1. Device schematic. The SIMS profile shows the concentration of Si and Fe in the dash box vertically.

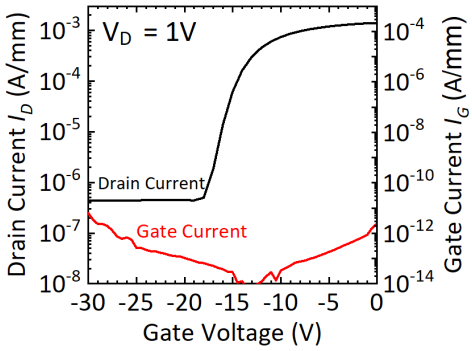

Fig. 2. The transfer characteristics at V_D =1V.

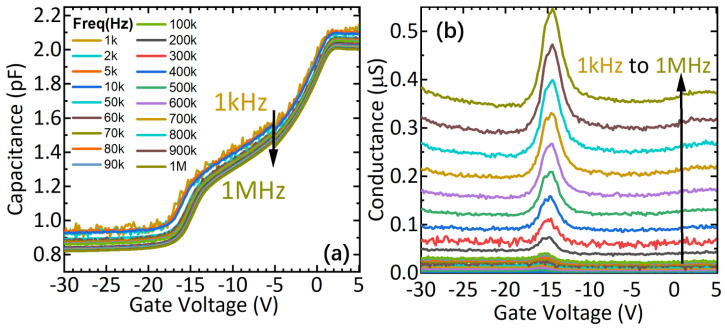

Fig. 3. (a) Gate-to-source capacitance and (b) corresponding equivalent conductance of the test devices at various frequency (1k-1MHz). The discontinuity of the capacitance around -5V is an artifact of the equipment.

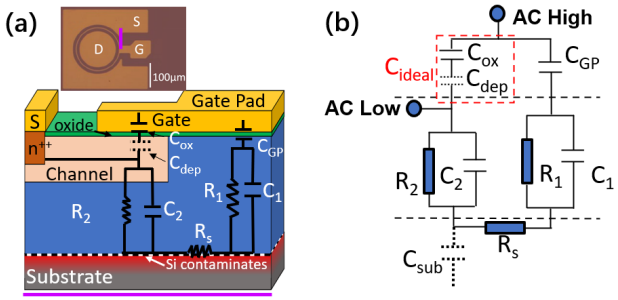

Fig. 4. (a) Schematic of coupling model when measuring gate-source impedance. (b) corresponding equivalent circuit.

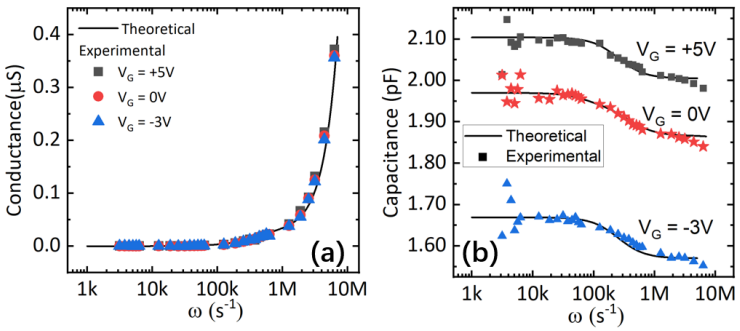

Fig. 5. (a) and (b) demonstrate the comparison of experimental results at V_G = +5V, 0V, and -3V and fit of models. The fitting parameters are listed in Table I.

Table I. The values of the elements obtained from the fitting

V_G(V)	+5	0	-3
C_{ideal} (F)	2.0E-12	1.9E-12	1.6E-12

C_{GP} (F)	R_1 (Ω)	C_1 (F)	R_2(Ω)	C_2(F)	R_s(Ω)
8.6E-12	4.0E7	2.2E-12	7.0E4	1.1E-13	5.5E3