Heterogeneous Material Integration
Room Bansal Atrium - Session HM-TuP

Heterogeneous Material Integration Poster Session II

HM-TuP-1 Bond-and-Thin Process for Making Heterogeneous Substrate with a Thin Ga_2O_3 Layer om Polycrystalline SiC Substrate, ***Alex Usenko**, A. Caruso,* University of Missouri-Kansas City*; S. Bellinger,* Semiconductor Power Technologies

Making Power Semiconductor Devices on starting heterogeneous engineered substrates gives numerical advantages over making them on bulk blanket wafers.

For β-Ga_2O_3 it allows to mitigate its critical disadvantage – low thermal conductivity that heavily limits its applications to power semiconductor devices.

In our process flow, we bond 100 mm cmmercially available polycrystalline SiC wafer to 100 mm commercially available β-Ga_2O_3 wafer using room temperarature surface activation bonding process. Then we thin the initial β-Ga_2O_3 to a mnimum thickness needed for desired device voltage.

As each micron of β-Ga_2O_3 withstand up to 800V, the typical final thickness is several microns.

Using polycrystalline SiC substate is for 2 reasons - it is more than 10X cheaper than single crystalline one, and it can have 100X lower electricall resistance compared to aregular nitrogen doped SiC. Indeed, the substrate here is just mechanical support and electrical contact, no semiconductor properties needed. For processes based on epitaxial growth - crystalline lattice is needed, while our process - wafer bonding - is independent on crystal structure.

Next we etch the continuous β-Ga_2O_3 layer into islands equal in shape and area to future power chips to be made on them. Reason is, the continuous layer will not withstand ~1000C processing steps for making MOSFETS and even Schottky diodes. The continuous layer breaks due to difference in thermal expansion. While the islands withstand the thermal processing. The process is being patented.

HM-TuP-3 Design of 10 kV P-Diamond/I-Ga_2O_3/N-Ga_2O_3 Power PN Diodes, ***Hunter Ellis**, K. Fu,* Department of Electrical and Computer Engineering, University of Utah

β-Ga_2O_3 is a promising ultra-wide bandgap semiconductor material with a unique combination of ultra-wide bandgap, high breakdown field, and large wafer size [1]. Devices based on β-Ga_2O_3 are expected to be smaller, cheaper, more efficient, and more temperature- and power-resistant than other semiconductors [1,2]. However, several obstacles stop β-Ga_2O_3 from being a mainstream electronics material. Specifically, the lack of effective P-type dopants and low thermal conductivity pose significant challenges [1,3]. Since a PN junction is the basic building block for device design, the absence of P-type β-Ga_2O_3 has prevented the full exploitation of its properties, and conventional device design strategies used for Si cannot be transferred to β-Ga_2O_3. On the other hand, high thermal conductivity is critical in electronic devices to minimize heat damage and reduce the likelihood of failure [1, 3].

A P-type diamond and N-type Ga_2O_3 PN heterostructure could address these issues. Diamond could form an ideal heterojunction with β-Ga_2O_3 due to their ultra-wide bandgaps. Diamond is relatively easy to make P-type and has high thermal conductivity; a simulated PN junction is shown in the supplemental document [3,4]. This structure can simultaneously address both problems. However, significant work in device design and integration of epitaxial growth is needed to realize this concept.

In this study, we established a model for the PN heterojunction. We investigated the energy band diagram for the P-diamond/I-Ga_2O_3/N-Ga_2O_3 structure, edge termination to mitigate electric field crowding, drift layer design (I-Ga_2O_3) to increase the breakdown voltage and reduce the on-resistance, and temperature dependence. We successfully designed 10 kV P-diamond/I-Ga_2O_3/N-Ga_2O_3 power PN diodes, and the results are very promising for this type of ultra-wide bandgap PN heterojunction. Effects of interface states on device performance were also investigated due to the importance of epitaxial growth.

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[4] P. Sittimart, S. Ohmagari, T. Matsumae, H. Umezawa, and T. Yoshitake, "Diamond/β-Ga_2O_3 pn heterojunction diodes fabricated by low-temperature direct-bonding," *AIP Advances,* vol. 11, no. 10, p. 105114, 2021.

HM-TuP-5 Heterogeneous Material Integration, ***Yash Mirchandani**,* Syrnatec

The use of UWBGs (Ultra-Wide Bandgap Semiconductors) based power converters is an emerging technology that will revolutionize power electronics industries.Space-rated DC-DC converters' performance and power density are primarily limited by high-power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Power MOSFETs are very susceptible to damage and degradation from the irradiation found in space, especially ionizing radiation. As a response to the current technology gap, Syrnatec in collaboration with University at Buffalo has developed a revolutionary Ga2O3 technology-based UWBGs. These Ga2O3 MOSFETs are capable of demonstrating more robustness to single event effects than their rad-hard power MOSFET counterparts. Because Ga2O3 MOSFETs do not have a metal oxide layer, they are very robust to ionizing radiation, which prevents charge entrapment from TID in high radiation environments. After exposure to 500 krad (Si) ionizing doses, early radiation tests on first generation Ga2O3 MOSFETs showed less than 4% threshold voltage variation (VTH) and less than 3% RDSON change. When the devices were in the OFF state, higher variation was reported (18% VTH and 8% RDSON). In second generation Ga2O3 MOSFETs, no performance degradation has been observed from TID to 1.0 Mrad (Si).Syrnatec's Gallium Oxide MOSFET, an upcoming wide bandgap material that is not only inherently radiation tolerant, but is also suitable for operating in environments with extreme temperatures such as lunar night, where the temperature changes from -153 degrees Celsius to 123 degrees Celsius , and -125 degrees Celsius to 80 degrees Celsius.

Syrnatec will incorporated its Ga2O3 technology into DC-DC converters with a bulk voltage of 20% to 80% and a trickle voltage of above 80%. With a maximum and minimum bulk charge timer (validated as the charge parameters), a Trickle voltage per cell (to be 2V), Boost and trickle voltage settings (Boost is 120% of the rated voltage, Trickle is 2V) and a Device switch off setting (tested on a battery under 20%). With no errors in over voltage and over current test conditions at 150% rated input for 1 sec out of every 10 seconds while maintaining an average of 100% overall rated values for the other 9 seconds. In addition, we have evaluated the success of fault detection across the entire Military Grade Temperature flow. In both buck and boost modes, power conversion efficiency exceeded 96% over the entire temperature range.

Overall, Ga2O3 based power converters can bring several novel features to the US commercial market, including high breakdown voltage, high thermal conductivity, wide bandgap, and low cost.

HM-TuP-6 Si/Ga_2O_3 and GaAsP/Ga_2O_3 P-N Diodes via Semiconductor Grafting, *J. Zhou, D. Kim, H. Jang, Q. Lin, **Jiarui Gong**,* University of Wisconsin - Madison*; F. Alema, A. Osinsky,* Agnitron Technology Inc.*; K. Chabak, G. Jessen,* Air Force Research Laboratory*; S. Pasayat,* University of Wisconsin - Madison*; C. Cheung, V. Gambin,* Northrop Grumann*; C. Gupta, Z. Ma,* University of Wisconsin - Madison

Ga_2O_3, an ultrawide-bandgap semiconductor, has attracted substantial attention in recent years due to its exceptional electronic properties and its vast potential in power electronics and solar-blind optoelectronics [1]. Despite these attractive properties of Ga_2O_3, there are some challenges to be addressed. For instance, the long-standing issue of lack of p-type doping in Ga_2O_3 has persisted [2]. The inefficiency stems from high ionization energy of acceptors when using the common dopants in Ga_2O_3. As a result, the design and fabrication of high-performance bipolar Ga_2O_3 devices, such as p-n diodes, and HBTs, are still in the research and development stage.

Semiconductor grafting [3], which enables the formation of heterostructures between two arbitrary monocrystalline semiconductors, could be the approach to overcoming the current constraints through the creation of Ga_2O_3 heterostructures, wherein a foreign semiconductor with good p-type doping to integrate with Ga_2O_3 at the atomic level. In this approach, an ultrathin oxide (UO) layer at sub-nanometer scale serves both as the interfacial passivation layer and an effective quantum tunneling layer. In the present case, the surface Ga_2O_3 layer and the possible native oxide of Si should have played the role of the UO layer in the grafting approach.

Employing the semiconductor grafting technology, two types of Ga_2O_3 heterojunctions are created, including Si/Ga_2O_3 and $GaAsP/Ga_2O_3$, to address the current challenges of ineffective p-type doping in Ga_2O_3 and lack of bipolar devices. In these two structures, p-type Si and p-type GaAsP nanomembranes (NM) are released from their respective epi substrates, transfer-printed and then subsequently chemically bonded to the n-type Ga_2O_3 substrates, forming PN abrupt heterojunctions, and the grafted heterostructures were subsequently fabricated into PN diodes. Their respective diode schematics are shown in Figs. 1 (a) and (b), with preliminary I-V curves for both diodes displayed in Figs. 1 (c) and (d). Both Si/Ga_2O_3 and $GaAsP/Ga_2O_3$ exhibit excellent rectifying behaviors with rectification ratios of 10^7 and 10^3 at ±2V, respectively. Meanwhile, their ideality factors are characterized to be 1.13 for Si/Ga_2O_3 diode and 1.35 for $GaAsP/Ga_2O_3$ diode.

In conclusion, we have demonstrated the feasibility to fabricate Ga_2O_3 bipolar devices via the semiconductor grafting approach. The demonstration of the high-performance Si/Ga_2O_3 and $GaAsP/Ga_2O_3$ PN diodes could lead to functional Ga_2O_3 HBTs in the near future.

References:

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