Material and Device Processing and Fabrication Techniques Room Bansal Atrium - Session MD-TuP

Material and Device Processing and Fabrication Techniques Poster Session II

MD-TuP-1 Growth of Room Temperature Polycrystalline β-Gallium Oxide Thin Film, ***Damanpreet Kaur***, *M. Kumar,* Indian Institute of Technology Ropar, India

Gallium oxide as an ultra-wide band gap semiconductor can exist in five different polymorphs – α, β, γ, κ, and ε – with different crystal structures and slightly different band gaps in the range of 4.6-5.3 eV.[1] The β-Ga_2O_3 is the most stable and most widely studied phase with intrinsic solar-blindness, band gap of 4.8 eV, high chemical and thermal stability, high breakdown voltage and high radiation hardness. Most of the existing literature have reported the fabrication of crystalline β-Ga_2O_3 at elevated temperatures (> 300°C) with no report on room temperature crystallization of gallium oxide.[2, 3] The material is either grown at a high temperature or it is annealed for achieving crystallization. The room temperature growth of gallium oxide is often reported to be amorphous in nature.

Herein, we report the formation of good quality polycrystalline β-Ga_2O_3 on *c*-plane sapphire at room temperature via RF Magnetron Sputtering. Grazing incidence X-ray Diffraction scans in the ϑ-2ϑ mode shows the peaks corresponding to the formation of polycrystalline peaks of β-Ga_2O_3. There is a shift in the peaks implying a strain in the films. Atomic Force Probe microscopy images reveal the formation of large grains which might be the cause of the strain in the films grown at room temperature. As a simple proof of concept, a photodetector with interdigitated Au electrodes was fabricated which showed a low dark current (~ 8 nA at +5 V) and a two order of magnitude (~ 0.46 μA at +5 V) enhancement upon 254 nm illumination.

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MD-TuP-2 Performance and Traps of Ga_2O_3 Schottky Barrier Diodes with Mesa Structure, ***Min-Yeong Kim***, NIST-Gaithersburg, Republic of Korea; *O. Maimon,* NIST-Gaithersburg; *N. Hendricks, N. Moser,* Air Force Research Laboratory, USA; *S. Pookpanratana,* NIST-Gaithersburg; *S. Koo,* KwangWoon University, Korea; *Q. Li,* George Mason University

Among the ultrawide bandgap materials, Ga_2O_3 is expected to surpass the trade-off relationship between breakdown (BV) and on resistance ($R_{on,sp}$). However, the Ga_2O_3 vertical Schottky barrier diode (SBD) still cannot achieve the theoretical breakdown electric field. To improve electric field management, device designs incorporating field rings, junction termination extension, field plates, and mesa structure could be used to reduce the leakage current in the reverse bias state. The edge termination technique has been demonstrated to extend the breakdown voltage close to the ideal value that is determined by the material properties.[1] Fabricating mesa structures for edge termination can introduce defects and charge traps. Deep level traps can negatively affect the performance of devices by trapping charge carriers, resulting in reduced minority carrier lifetime and increased leakage current.

Here, we analyzed the characteristics of Ga_2O_3 SBDs with and without the mesa structure. The SBDs were fabricated on Si-doped β-Ga_2O_3 grown by halide vapor phase epitaxy (HVPE) on a Sn-doped ($6x10^{18}$ cm^{-3}) (001) β-Ga_2O_3 substrate. In the SBD with mesa structure, the circular mesa with a diameter of 162 μm and a depth of 500 nm was formed around anode electrodes. The Ti/Au metal stack on the polished back side of the substrate acted as a cathode while Ni/Au/Pt layers on the epitaxy acted as the anode electrode. After the fabrication process, current-voltage (I-V) measurements were performed as shown in Figure 1a. From the results, the $R_{on,sp}$ at 1 V are 6.9 Ω•cm^2 and 7.9 Ω•cm^2 in planar and mesa SBDs, respectively. In addition, the leakage current at -165 V is reduced by approximately 99.9% in the mesa structure. Figure 1 (b) shows the reverse bias characteristics of the SBDs, where the SBDs with mesa structure have approximately 2.75 times higher BV than SBDs without a mesa structure. Deep level defects were investigated by deep level transient spectroscopy (DLTS), and the SBDs with different structure have similar trap energy levels shown in Figure 2. In general, the trap density is larger in the SBD with mesa structures, however, the trap near the 3.0 eV is only detected for the SBD without the mesa structure and this defect is related to surface contamination. [2] Furthermore, we will extend the study by performing the cathodoluminescence (CL) spectroscopy to get radiative defect information of the SBDs which could be related to the DLTS results. We will discuss these results in light of the enhanced electrical performance of SBDs with mesa structures.

MD-TuP-4 Evolution of Lattice Distortions Throughout Various Stages of (010) β-Ga_2O_3 Substrate Preparation, ***Michael Liao***, National Research Council Postdoctoral at the U.S. Naval Research Laboratory; *N. Mahadik,* Naval Research Laboratory; *R. Lavelle, D. Snyder, W. Everson, D. Erdely, L. Lyle, N. Alem, A. Balog,* Penn State University; *T. Anderson,* Naval Research Laboratory

Meticulous preparation of substrates – in particular chemical mechanical polishing – is vital to many subsequent processes such as epitaxial growth, device fabrication and wafer bonding. After slicing substrates from boules, the rough substrates require lapping and polishing to achieve surfaces for epitaxial growth. However, lapping and aggressive polishing introduce sub-surface damage even if smooth surfaces are achieved.[1] Sub-surface damage manifests itself as lattice distortions such as tilt and strain, as well as generation of extended defects. The lattice distortions can be assessed using X-ray diffraction along different scanning axes. Previous work has been done to optimize polishing parameters to simultaneously achieve smooth (< 0.5 nm rms roughness) and subsurface-damage-free substrates.[2] Interestingly, it was found that the damage induced by wafer slicing was not only predominately lattice tilt, but the tilt was preferentially oriented along the [100] crystallographic axis. In this current work, we investigate the evolution of sub-surface damage of Czochralski-grown (010) β-Ga_2O_3 wafers that have undergone various preparation stages: wire sawn surfaces, lapping, and final polished surfaces. Multiple asymmetric reciprocal space maps (RSM) in the glancing incidence geometry were measured along different zone axes to deconvolve the contributions of lattice tilt and strain from sub-surface damage. For the wire sawn rough surface, the (420) RSM shows ~2.4× higher broadening along the ω-scanning axis, which is an indication that the nature of lattice distortion is predominately lattice tilt. Furthermore, this broadening was asymmetrical, which is an indication that the lattice tilt is anisotropic and could be related to the anisotropic elastic properties for various β-Ga_2O_3crystal planes. This was in contrast to the polished sample, where the distortion due to tilt was mostly removed, and there exists significantly reduced residual strain, indicated by small broadening in the ω:2θ scanning axis. These results are analyzed using the theoretical calculations of β-Ga_2O_3 elastic properties[3] to obtain insight on its unusual response to mechanical deformation during the wafer slicing and lapping process.

This research was performed while M.E.L. held an NRC Research Associateship award at the U.S. Naval Research Laboratory.

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MD-TuP-5 Investigation of In-Plane Anisotropy of In-situ Ga etching on (010) β-Ga_2O_3, ***Abishek Katta***, Arizona State University; *F. Alema, W. Brand, A. Osinsky,* Agnitron Technologies; *N. Kalarickal,* School of Electrical, Computer and Energy Engineering, Arizona State University

We report on 'in-situ' MOCVD Ga etching using the metal organic Ga precursor triethylgallium (TEGa) and the in-plane anisotropy of the etch characteristics. Etch rates exceeding 8μm/hr is demonstrated at high TEGa flow rates and a substrate temperature >900°C. Significant in-plane anisotropy in etching is observed on (010) β-Ga_2O_3 samples with trenches formed along [001] direction showing the smoothest sidewalls.

Many promising device structures used in Ga_2O_3, like trench SBDs, trench MOSFETs, FinFETs etc require fabrication of 3-D structures like fins and trenches. Several etch techniques have been reported, including ICP-RIE, wet etching and metal assisted chemical etching. However, most of these

techniques result in angled sidewalls and surface damage. Previously, exposure to metallic Ga was shown as a promising technique for etching Ga_2O_3, using the suboxide reaction 4Ga (s)+ Ga_2O_3 (s)—>3Ga_2O(g). In this work, we show that the suboxide reaction can also proceed by using TEGa as the Ga source with the Ga_2O_3 samples held at high temperature inside an MOCVD reactor.

The etching experiments were carried out in an Agnitron Agilis 100 MOCVD oxide reactor with a far injection showerhead. The variation in etch rate as a function of substrate temperature and TEGa flow rate was studied. Etch rate increases with substrate temperature till 900°C, above which no significant increase is observed. The etch rate also increases linearly with TEGa flow rate, eventually saturating at high flow rates. At T_{sub}=900°C and 1000°C, etch rates exceeding 8µm/hr is obtained, making it possible to fabricate deep trenches and high ASR 3-D structures. We also investigated in-plane anisotropy by using spoke wheel structures patterned on (010) β-Ga_2O_3 substrate (see Fig.2). The spoke wheel structure was etched at T_{sub}=800°C and TEGa flow rate of 12.1µmol/min to vertical etch depth of 2.5µm. In addition to vertical etching, lateral etching of the trenches was also observed, resulting in widening of the final trench widths. Using the final and initial trench widths, the ratio of lateral to a vertical etch rate was measured for various in-plane orientations on (010) β-Ga_2O_3. The lateral etch rate was found to be lowest for trenches oriented in the [001] direction (forms (100) sidewalls) and highest for fins oriented in the [102] directions (forms (-201) sidewalls). The trenches were also found to have vertical sidewalls which are ideal for fabricating sub-micron structures. The trench sidewalls along most orientations were found to be rough, however smooth sidewalls are obtained along [001] direction.

MD-TuP-6 Understanding Ohmic Contacts to N+ Doped (010) β-Ga_2O_3 by Both In-Situ MOCVD Doping and Silicon Ion Implantation, ***Kathleen Smith***, *K. Gann, C. Gorsak, N. Pieczulewski, H. Nair, M. Thompson, D. Jena, H. Xing,* Cornell University

Despite the promising properties of β-Ga_2O_3 for kV radio frequency (RF) applications, such as the large bandgap and critical electric field, decent carrier mobility, and availability of native substrates via many melt-growth techniques, Ga_2O_3 faces similar challenges to many wide bandgap semiconductors. Namely, the low electron affinity associated with the wide bandgap leads to few low work-function metals to form ohmic metal-semiconductor junctions. Instead, Ga_2O_3 relies on tunnel junctions between a metal and heavily doped regions for ohmic behavior. However, the reliable formation of such junctions is non-trivial.

In order to enable high speed device applications, the parasitic resistance from the contacts R_c should be much less than 1 Ω-mm. In this work, we demonstrate ohmic contacts well below this threshold both for ion-implanted and metal-organic chemical vapor deposition (MOCVD) grown heavily doped (N_d > 1E19 cm^{-3}) Ga_2O_3. We also show the resultant R_c can depend on subtle differences in Ga_2O_3 surface properties.

Ion-implanted samples were prepared by implanting Si into a 400 nm unintentionally doped epitaxial layer grown on an Fe-doped (010) β-Ga_2O_3 substrate to a box concentration of 5x10^{19} cm^{-3} over 100 nm, activated by a 20 minute anneal at 950 °C in dry UHP nitrogen. Transfer length method (TLM) patterns were then formed with Ti/Al/Ni (50/100/60 nm) ohmic contacts. The contacts were then alloyed by a series of rapid thermal anneals (RTA) in nitrogen ambient. The resulting TLM patterns had an R_c of 0.16±0.01 Ω-mm, and a sheet resistance R_{sh} of 237±2 Ω/□.

Heavily doped samples were also grown on Fe-doped (010) β-Ga_2O_3 via MOCVD, with in situ Si doping to a nominal concentration of 9x10^{19} cm^{-3} and a thickness of 150 nm. TLM patterns were made with Ti/Au (50/110 nm) contacts, and compared before and after post-contact deposition RTA. On some MOCVD samples, the unalloyed contacts show an extremely leaky Schottky behavior, with a measured R_c of 0.35±0.002 Ω-mm and an R_{sh} of 55±1 Ω/□ at a current bias of 50 mA. On others, the unalloyed contacts show a highly rectifying behavior. These also become ohmic post annealing; however, the resultant contacts were found to be extremely non-uniform spatially. We currently ascribe these abnormal contacts to the formation of a spatially non-uniform interfacial layer on the Ga2O3 surface. While these results demonstrate the attainability of low R_c, future efforts will be needed to carefully control the surface properties to reliably achieve low R_c and apply these contacts to the moderately doped channels desired for kV RF applications.

MD-TuP-7 Heteroepitaxial Growth of $ZnGa_2O_4$ by Post-Deposition Annealing of ZnO on Ga_2O_3 Substrate, ***Stefan Kosanovic***, *K. Sun,* University of Michigan, Ann Arbor*; U. Mishra,* University of California Santa Barbara*; E. Ahmadi,* University of Michigan, Ann Arbor

In recent years, β-Ga2O3 has attracted a great deal of interest for the next generation of power electronics due to its ultra-wide bandgap (~4.6 eV) and availability of native substrates. Spinel ZnGa2O4 is another ultra-wide bandgap semiconductor with similar bandgap (~4.6-5 eV) as Ga2O3. Moreover, in ternary spinel oxides, cations occupy octahedral and tetrahedral sites formed by oxygen atoms, leading to new possibilities for doping. Recent studies suggest that p-type doping in spinel ZnGa2O4 may be possible [1-3] Therefore, a Ga2O3-ZnGa2O4 heterostructure may enable design and fabrication of novel devices.

Several methods including sol-gel, RF magnetron sputtering, pulsed laser deposition, metalorganic chemical vapor deposition (MOCVD), and mist-CVD have been previously used for epitaxial growth of ZnGa2O4 on foreign substrates such as sapphire. Bulk ZnGa2O4 single crystal has also been fabricated using melt growth techniques [4]. Here we demonstrate a novel method for heteroepitaxial growth of high quality ZnGa2O3 on Ga2O3 substrate. In this method ZnO is first deposited by ALD on Ga¬2O3 followed by annealing at 900 C. TEM images revealed high structural quality of the film and a well-defined interface. SAED images showed that the ZnGa2O4 “semi-concurrently” matched to the Ga2O3 substrate, supporting high film quality. These results are demonstrated for the (-201), (001), and (010) Ga2O3 orientations.

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MD-TuP-8 Revitalizing Fractured β-Ga_2O_3 Nanomembranes: Nanogap Recovery for Enhanced Charge Transport Performance, *M. Hasan, J. Lai,* ***Jung-Hun Seo***, University at Buffalo

A free-standing β-Ga_2O_3, also called β-Ga_2O_3 nanomembrane, is an important next-generation wide bandgap semiconductor that can be used for myriad high-performance future flexible electronics. However, details of structure-property relationships of β-Ga_2O_3 NM under strain conditions have not yet been investigated. In this presentation, we systematically investigated the electrical properties of β-Ga_2O_3 NM under different uniaxial strain conditions using various surface analysis methods and revealed layer-delamination and fractures. The electrical characterization showed that the presence of nanometer-sized gaps between fractured pieces in β-Ga2O3 NM caused a severe property degradation due to higher resistance and uneven charge distribution in β-Ga_2O_3 NM which was also confirmed by the multiphysics simulation.

The degraded performance in β-Ga_2O_3 NM was substantially recovered by two different methods. (i) Saturated water vapor treatment: introducing excessive OH-bonds in fractured β-Ga_2O_3 NM via the water vapor treatment. The X-ray photoelectron spectroscopy study revealed that the formation of OH-bonds by the water vapor treatment chemically connected nano-gaps. (ii) Oxide passivation: deposition of a thin oxide layer such as Al_2O_3, HfO_2, and SiO_2 that is formed by an atomic layer deposition (ALD) system allows charges for hopping across fractured β-Ga_2O_3 pieces.

The treated β-Ga_2O_3 samples by the aforementioned method exhibited reliable and stable recovered electrical properties up to ~90 % of their initial values. Therefore, this result offers a viable route for utilizing β-Ga_2O_3 NMs as a next-generation material for a myriad of high-performance flexible electronics and optoelectronic applications.

MD-TuP-9 Impact of Magnetron Sputtered Ultra-Thin Layer of Fe-Doped β-Ga_2O_3 on Gallium Oxide Schottky Contacts, ***Adetayo Adedeji,*** Elizabeth City State University*; J. Merrett,* Air Force Research Laboratory, Aerospace Systems Directorate*; J. Lawson, C. Ebbing,* University of Dayton Research Institute

Adetayo Victor Adedeji[1], Jacob Lawson[2], Charles Ebbing[2], J. Neil Merrett[3]

[1] Elizabeth City State University, [2] University of Dayton Research Institute, [3] Air Force Research Laboratory

Ultra-thin layer (~ 4 nm) of Fe-doped ß-Ga_2O_3 was deposited by co-sputtering pure Ga_2O_3 and Fe targets on (010) n+ Sn-doped Ga_2O_3 epilayer grown by Halide Vapor Phase Epitaxy (HVPE) on Si-doped ß-Ga_2O_3 substrates. The HVPE epilayer was about 4.5 mm thick and 2E16 cm^{-3} doping concentration. The ultra-thin insulating layer was deposited at 600°C substrate temperature for 10 minutes in Ar/O_2 gas mixtures (5% O_2 by flow rate). 100W RF power was applied to the Ga_2O_3 target while the dopant target was sputtered with 9W DC power. Circular Ti contacts were deposited on a 5 mm x 5 mm sample by photolithography and magnetron sputtering. The sample was annealed in argon flow at 400°C after contact metallization. The I-V characteristics of the Schottky diodes showed that the reverse current of samples with ultra-thin Fe-doped ß-Ga_2O_3 is more that five orders of magnitude lower than samples without the ultra-thin layer while the forward current dropped by about one order of magnitude. Appreciable forward bias tunneling current was achieved with much lower reverse current compared with samples without insulating nanolayer. It has been demonstrated that this technique can be used to tune the barrier height of Schottky contacts to ß-Ga_2O_3. Such low leakage contacts can be useful in improving the performance of metal-semiconductor gates in MESFETs or in reducing the edge leakage of Schottky power diodes.

MD-TuP-10 An Investigation of (001) β-Ga_2O_3 Etching via Heated H_3PO_4, ***Steve Rebollo,*** *T. Itoh, S. Krishnamoorthy, J. Speck,* University of California, Santa Barbara

The fabrication of power devices that approach the β-Ga_2O_3 unipolar-FOM limit requires the use of field-management and RESURF techniques.[1] Utilizing dry etch processes for these techniques results in defect formation, which can impact the performance of devices.[2] Recently, Yuewei et al. used a wagon wheel pattern to explore the anisotropic etching behavior of (010) β-Ga_2O_3 in heated H_3PO_4. Compared to (010) β-Ga_2O_3, the (001) orientation is a better candidate for vertical power devices due to improved substrate scalability and slightly higher

PECVD was used to blanket deposit 533 nm of SiO_2 on Ga_2O_3. A wagon wheel pattern with 25 µm spoke widths was defined using photolithography. The spokes oriented along the [100] and [010] directions were carefully aligned to the edges of the substrates, which correspond to the (100) and (010) planes, respectively. Photoresist served as a mask to protect the SiO_2 during an HF etch. The SiO_2 etch rate was determined using Si substrates that were coloaded in the PECVD with the Ga_2O_3 substrate. Next, the sample was placed in a H_3PO_4/H_2O solution for 3.2 hours at a temperature of 140°C. The temperature was monitored and controlled using a temperature probe. The etch depth was determined via profilometry. Afterward, the sample was characterized via SEM.

Figure 1 shows an SEM image of the wagon wheel post-etch. The SiO_2 mask protecting the top of the spokes is still intact. Figure 2 shows a profile of the wagon wheel after etching. Assuming no significant SiO_2 etching[2], the (001) etch rate is 781 nm/hr. Figure 3 shows a 60°-tilted SEM image of a spoke oriented along the [-100] direction. An undercut of the SiO_2 mask can be observed. Since (010) is a mirror plane in β-Ga_2O_3, the spoke is symmetric about the (010) plane. Figure 4 shows the sidewall angles for the wagon wheel spokes. For spokes with an orientation in a positive k-direction, the right-hand sidewalls of the spokes were smooth and had low inclination angles and the left-hand sidewall exhibited roughness with a steeper inclination angle. The opposite was true for spokes oriented in the negative k-direction. This is another consequence of the mirror plane symmetry. The roughness could be the result of rough SiO_2 mask sidewalls. These findings can be useful for the development of dry-etch free process flows for high-performance devices.

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MD-TuP-11 An Organic, Direct Bonded Copper, Multi-Layered, Ultra-Low Inductance Package for High-Power UWBG MOSFETs, *J. Major, J. Calder, S. Zhao,* ***Faisal Khan,*** National Renewable Energy Laboratory

The most common metalized substrates used in high-power switching packages consist of a ceramic layer such as Aluminum Nitride (AlN) sandwiched between two copper layers. Ceramic substrates are used because it has the key characteristic of having high dielectric strength while being thermally conductive. A large drawback to ceramic substrates is that they do not allow for a multi-layered circuit design. By replacing the traditional ceramic substrate with organic direct bonded copper (ODBC) we can open a wide range of possibilities when it comes to power module layout such as multi-layered circuits and double-sided cooling. Both benefits are critical while packaging high-performance Gallium Oxide (Ga_2O_3) MOSFETs. Because of Ga_2O_3's relatively poor thermal conductivity, a double-sided cooled package becomes necessary. Therefore, the use of ODBC provides the flexibility to fabricate copper traces carrying much higher currents, and by creating a multi-layered package, we can drastically reduce the parasitic inductance inside the power module. Achieving lower parasitic inductance is critical for an ultra-fast Ga_2O_3 package to avoid excessive voltage overshoot and ringing. Using ODBC, we have designed novel packages capable of handling the challenges presented by fast Ga_2O_3 switching. Using multi-physics modeling software, we can validate our design before building the prototype. Due to the simple process parameters needed to work with ODBC, we can rapidly create prototypes without using external vendors. This flexibility allows us to quickly design, build, and validate highly complex switching power modules to accommodate next generation, Ga_2O_3 switching devices.

Author Index

Bold page numbers indicate presenter