Program Overview

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Electronic Transport and Breakdown Phenomena
Room Jefferson 1 & Atrium - Session ET-MoP

Electronic Transport and Breakdown Phenomena Poster Session

ET-MoP-2 Electric Field Mapping in β-Ga_2O_3 by Photocurrent Spectroscopy, ***Darpan Verma**, M. Adnan, S. Dhara,* Ohio State University; *C. Sturm,* Universitat Leipzig, Germany; *S. Rajan, R. Myers,* Ohio State University

Power electronics devices suffer from unexpected field non-uniformity, and high field often degrades these devices by limiting their lifetime. Electric-field mapping could aid in the design of device features non-destructively by identifying breakdown regions. We will discuss progress in developing an E-field mapping technique that can spatially map out the E-field maxima in β-Ga_2O_3 space charge regions and could identify E-field hotspots at which the breakdown is likely. Previously, we showed that the Exciton Franz-Keldysh (XFK) effect can be used to estimate the local E-field maximum in (010) β-Ga_2O_3 Schottky diodes based on the redshift of the photocurrent spectral peak.[1] In that study, we implemented an XFK model using an analytical approximation for the XFK effect based on the modified Wannier-Mott model. Here, we extend these measurements to higher photon energies (< 5.6 eV) in (001) β-Ga_2O_3 Schottky diodes, and observe a total of three absorption peaks whose intensity varies with the angle of the linear polarization of the monochromatic UV light incident on the device. The three peaks at 4.9 eV, 5.2 eV and at 5.5 eV, match quasi-particle-DFT transitions as well as measurements in β-Ga_2O_3 from previous studies[2,3]. Peaks at 4.9 eV and 5.2 eV correspond to excitons polarized within the a-c plane, and the peak at 5.5 eV corresponds to exciton along the b axes. These peaks red shift with bias and can be calibrated to serve as an E-field sensors. A well-calibrated vertical Schottky barrier diode was fabricated on a 10um thick HVPE grown (001) β-Ga_2O_3 epitaxial layer (N_D=1.5E16/cm^3). For the top Schottky contact, a circular Pt (5nm) layer was deposited by E-beam evaporation. Further, leaving the center of the Pt layer exposed for light illumination, a circular ring (overlapping the thin Pt layer) with a contact pad was fabricated using Pt/Au (30/70nm). Afterward, an ohmic back contact of Ti/Au (30/70nm) was blanket deposited. At this structure, the parallel-plate electric field can be theoretically estimated to calibrate the redshift of the photocurrent peaks to E-field values and convert the spatially-resolved photocurrent spectra into mapped E-field values across the whole device active region.

References:

[1] M.M.R. Adnan, D. Verma, Z. Xia, N.K. Kalarickal, S. Rajan, and R.C. Myers, Phys. Rev. Appl. **16**, 1 (2021).

[2] J. Furthmüller and F. Bechstedt, Phys. Rev. B **93**, 1 (2016).

[3] C. Sturm, R. Schmidt-Grund, C. Kranert, J. Furthmüller, F. Bechstedt, and M. Grundmann, Phys. Rev. B **94**, 1 (2016).

ET-MoP-3 Activation of Si, Ge, and Sn Donors in High-Resistivity Halide Vapor Phase Epitaxial β-Ga_2O_3:N, ***Joseph Spencer,*** Naval Research Laboratory/ Virginia Tech CPES; *M. Tadjer, A. Jacobs, M. Mastro, J. Gallagher, J. Freitas, Jr,* Naval Research Laboratory; *T. Tu, A. Kuramata, K. Sasaki,* Novel Crystal, Japan; *Y. Zhang,* Virginia Tech (CPES); *T. Anderson, K. Hobart,* Naval Research Laboratory

With an ultra-wide bandgap (4.8eV), high critical field (6-8MV/cm) and melt-growth capability, the popularity of Gallium oxide (GO) has surged within the material growth and electronic device fields. Even with an UWBG, dopants such as Si and Sn have been shown to be shallow donors (30 and 60meV, respectively) [1-2]. It has also been demonstrated that the addition of nitrogen acceptors allows for the UID level to fall as low as $10^{14}cm^{-3}$, extending the doping range of GO by over an order of magnitude [3,4]. The inclusion of N also results in a highly resistive current blocking layer (CBL) in GO due to the deep acceptor state formed by the N dopants. In this work we demonstrate how implanted donors can overcompensate the highly resistive GO:N CBL, resulting in highly conductive films while the unimplanted regions remain highly resistive.

Halide vapor phase epitaxial (HVPE) films were grown on semi-insulating (001) GO:Fe substrates. Prior works [5] characterized the films using Secondary ion mass spectroscopy (SIMS) to confirm the presence of the N acceptor and 9.2 µm thickness. C-V measurements showed a net free carrier concentration below the detectable limit of 10^{14} cm^{-3} (N_D-N_A). Lateral Schottky diodes showed breakdown voltages that surpassed 2kV for the resistive films [5].

Linear/circular transfer length method (LTLM/CTLM) and van der Pauw (VdP) structures were patterned for donor implantation. Si, Ge, and Sn donors were implanted with a box profile of 100nm at a dose of $3.3^{14}cm^{-2}$. Implanted donors were activated with a rapid thermal anneal (RTA) at 925C for 30min in N2. The LTLM/CTLM and VdP structures were isolated using an 800W BCl_3 reactive ion etcher for a 150nm etch. Ti/Au ohmic contacts were deposited followed by a contact anneal.

A contact resistance (R_c) of 1.2 Ωmm and 2.3 Ωmm for the Si and Sn implanted samples, respectively was measured from LTLM/CTLMs. Temperature dependent Hall effect measurements (15-300K) gave the sheet carrier concentration (n_s), sheet resistance (R_{sh}), and mobility (µ). Hall structures that did not receive implantation of the active region between the ohmic contacts could not be measured due to excessive resistance demonstrating retention of N doped film resistivity. Full implanted VdP structures were highly conductive and measurable. At 300K, the Si, Ge, and Sn doped samples achieved mobilities, sheet resistances, and sheet electron densities of 86, 71, and 59 cm2/Vs, 324, 941, and 1750 Ω/sq, and 2.25e14, 9.3e13, and 6.0e13 cm^{-2} respectively. The implant activation efficiency was found to be 66%, 28%, and 18% for Si, Ge, and Sn, respectively. See supplemental page for references.

Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 2-3 - Session EP1-WeM

Process & Devices III

Moderator: Uttam Singisetti, University of Buffalo, SUNY

9:15am **EP1-WeM-4 Remarkable Improvement of Conductivity in Β-Ga_2O_3 by High-Temperature Si Ion Implantation**, ***Arka Sardar**, T. Isaacs-Smith, S. Dhar,* Auburn University*; J. Lawson, N. Merrett,* Air Force Research Laboratory, USA

Monoclinic Beta Gallium Oxide (β-Ga_2O_3) is emerging as a promising wide bandgap semiconductor for high voltage electronics. Ion implantation is a key process for device fabrication as it provides a unique way to carry out selective area doping with excellent control. It has been demonstrated that Si implantation into (010) β-Ga_2O_3 at room temperature followed by annealing at ~1000°C, results in an activation efficiency (η)of 63% for Si concentrations up to ~5e19 cm^{-3}. However, for higher concentrations, a severe drop of the η to 6% occurs [1]. In this work, we demonstrate that high-temperature implantation can be used to significantly improve this for heavily implanted β-Ga_2O_3. In the case of SiC, implantation at > 500°C results in superior conductivity due to lower defect densities and better recrystallization after annealing [2]. Based on this, we performed room temperature (RT, 25°C) and high temperature (HT, 600ºC) Si implants into MBE grown 300 nm (010) β-Ga_2O_3 films with energies of 275 keV and 425 keV through ~110 nm Mo and ~30 nm Al_2O_3 layers; with a total of fluence of 2.4e15 cm^{-2} or 4.8e15 cm^{-2}. This was followed by annealing in flowing nitrogen at 970ºC for 30 minutes to activate the dopants. SIMS shows the Si profile is ~400 nm deep with an average concentration of ~6.0e19 cm^{-3} for the lower fluence samples, and expected to be ~1.2e20cm^{-3} for the higher fluence (SIMS ongoing). No significant difference in surface roughnesses were detected by AFM throughout the process. HRXRD shows structural defects after the implantation and partial crystallization recovery upon annealing, where the advantage was in favor of HT implantation. The ratio of the free electron concentration from Hall measurements and the total amount of Si in β-Ga_2O_3 was used to determine the activation efficiencies. For the lower fluence, the HT sample shows only a ~6% improvement of η over the RT sample. Remarkably, for the higher fluence, while the RT sample was too resistive for measurement, the HT sample had η close to 70%, with a high sheet electron concentration of 3.3e15 cm^{-2} and excellent mobility of 92.8 $cm^2/V\cdot s$ at room temperature. These results are highly encouraging for achieving ultra-low resistance heavily doped β-Ga_2O_3 layers using ion implantation, which will be discussed further in this presentation.

References:

[1]K. Sasaki et.al,, Appl. Phys. Express 6, 086502 (2013).

[2]F. Roccaforte, et. al, , Micro 2, 23 (2022).

Acknowledgments:

We acknowledge the support of the Department of Physics, Auburn University.

9:30am **EP1-WeM-5 Towards Lateral and Vertical Ga_2O_3 Transistors for High Voltage Power Switching**, ***Kornelius Tetzner**, J. Würfl, E. Bahat-Treidel, O. Hilt,* Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany*; Z. Galazka, S. Bin Anooz, A. Popp,* Leibniz-Institut für Kristallzüchtung (IKZ), Germany **INVITED**

Gallium Oxide (Ga_2O_3) power switching devices are expected to boost efficiency of power converters predominately operating at comparatively high bias voltage levels in the kV range. Thanks to the extraordinarily high energy band gap of 4.9 eV a high device breakdown strength of about 8 MV/cm is expected. Thus it is possible to efficiently utilize these properties for very compact power devices with aggressively minimized gate to drain separation. This enables low resistive on-state and low leakage off-state properties. Most Ga_2O_3 devices introduced so far rely on volume electron transport properties; only a few 2DEG devices have been demonstrated. In any case the values of electron mobility and saturation velocity in Ga_2O_3 crystals may depend on crystal orientation and did not yet reach properties being comparable to more developed wide band gap semiconductor families such as GaN and SiC. – Nevertheless the benefit of Ga_2O_3 devices relates to the combination of high breakdown field and electron transport properties and the resulting compact device design strategies are already getting competitive to existing power switching technologies.

The presentation will give an overview on the current status of lateral and vertical Ga_2O_3 devices with a special emphasis on results obtained at FBH and IKZ [1]. For both cases concepts for epitaxial layer structures and device designs suitable for reaching the targeted performance will be discussed especially in terms of breakdown voltage and channel current density. Critical points for device optimization such as type of gate recess in lateral transistors and concepts of critical electric field reduction in vertical transistors will be addressed.

[1] K. Tetzner, IEEE Electron Device letters, vol. 40, No. 9, (2019), pp. 1503 - 1506.

10:00am **EP1-WeM-7 Comparison of β-Ga_2O_3 Mosfets With TiW and NiAu Metal Gates for High-Temperature Operation**, ***Nicholas Sepelak,*** KBR, Wright State University*; D. Dryden,* KBR*; R. Kahler,* University of Texas at Dallas*; J. William,* Air Force Research Lab, Sensors Directorate*; T. Asel,* Air Force Research Laboratory, Materials and Manufacturing Directorate*; H. Lee,* University of Illinois at Urbana-Champaign*; K. Gann,* Cornell University*; A. Popp,* Leibniz-Institut für Kristallzüchtung, Germany*; K. Liddy,* Air Force Research Lab, Sensors Directorate*; K. Leedy,* Air Force Research Laboratory, Sensors Directorate*; W. Wang,* Wright State University*; W. Zhu,* University of Illinois at Urbana-Champaign*; M. Thompson,* Cornell University*; S. Mou,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; K. Chabak, A. Green,* Air Force Research Laboratory, Sensors Directorate*; A. Islam,* Air Force Research Laboratory, Sensors Directory

β-Ga_2O_3 offers a robust platform for operation of electronic devices at a high temperature because of its large band gap and low intrinsic carrier concentration. We have recently characterized the high temperature performance β-Ga_2O_3 field effect transistors using different gate metals in vacuum and air ambient at temperatures up to 500 °C.

The devices fabricated using TiW refractory metal gate and Al_2O_3 gate dielectric exhibited stable operation up to 500 ºC in vacuum and up to 450 ºC in air [1]. Transfer (I_{DS}-V_{GS}) characteristics of a device were measured at various temperatures in vacuum and air. Extracted I_{MAX}/I_{MIN} for the vacuum test reduced from ~10^4 to 10^2 as temperature was increased up to 500 ºC. During the vacuum characterization, the contact resistance remained unchanged at all temperatures and, therefore, device characteristics showed no degradation once devices were brought back to RT even after several hours of device operation at 500 °C in vacuum.

The devices, fabricated with Ni/Au gate metal and Al_2O_3 gate dielectric, exhibited stable operation up to 500 ºC in air [2]. The measured I_D-V_D characteristics showed no current degradation up to 450 ºC. At 500 ºC, the device exhibited a drop in I_D; however, device characteristics recovered once the device is brought back to RT, even after 20 hours of device operation at 500 °C.

For tests in air ambient, both Ni/Au and Ti/W devicesobserved an increase in current with temperature due to activation carriers from dopants/traps in the device, however, both exhibited $I_{MAX}/I_{MIN} < 10^2$ at 450 ºC because of contact degradation. The barrier height of ϕ_B~ 1.0 eV and 0.77 eV was calculated for the TiW/Al_2O_3 and the NiAu/Al_2O_3 interfaces, respectively using thermionic emission theory. Thought the values of ϕ_B for the Ti/W contacts was consistent with that expected from the work-function difference between TiW and Al_2O_3, the devices with Ni/Au yielded lower ϕ_B presumably due to the diffusion of Ni and the partial crystallization of the Al_2O_3 dielectric [3]. Our results suggest that with appropriate choice of metals and gate dielectrics, the stable 500 ºC operation using β-Ga_2O_3 is achievable.

[1] Sepelak *et al*., "High-temperature operation of β-Ga_2O_3 MOSFET with TiW refractory metal gate," *DRC, 2022*.

[2] Sepelak *et al*., "First Demonstration of 500 °C Operation of β-Ga_2O_3 MOSFET in Air," *CSW, 2022*

[3] Islam et al., "Thermal stability of ALD-grown SiO2 and Al2O3 on (010) β-Ga2O3 substrates," DRC, 2022.

10:15am **EP1-WeM-8 High Electron Mobility Si-doped β-Ga_2O_3 MESFETs**, ***Arkka Bhattacharyya,*** University of Utah*; S. Roy,* University of California at Santa Barbara*; P. Ranga,* University of Utah*; S. Krishnamoorthy,* University of California at Santa Barbara

A hybrid low temperature - high temperature (LT-HT) buffer/channel stack growth is demonstrated using MOVPE with superior carrier mobility values. An LT-grown (600°C) undoped Ga_2O_3 buffer (250-330 nm thick) is grown followed by transition layers to a HT (810°C) Si-doped Ga_2O_3 channel layers (~220 nm) without growth interruption. The (010) Fe-doped Ga_2O_3 substrates were cleaned in HF for 30 mins prior to channel growth. From Hall measurements, this stack design is shown to have an effective RT Hall mobility values in the range 162 – 184 cm^2/Vs for doped channel electron densities of 1.5-3.5×10^{17} cm^{-3} measured on multiple samples/substrates. These mobility values are higher than the state-of-the-art values in Ga_2O_3 literature. Two types of (010) Fe-doped Ga_2O_3 bulk substrates were used in this study: 5×5 mm^2 diced pieces from 10×15 mm^2 EFG-grown substrates from NCT, Japan and 2-inch CZ-grown bulk substrates from NG Synoptics, USA.

The charge and transport properties were also verified using CV, TLM, field-effect mobility (μ_{FE}) measurements and FET current characteristics. Few samples were processed for regrown ohmic contacts to minimize contact resistance. R_C values of 1-2 Ω.mm were achieved. 3D electron densities were verified by CV measurements. Channel charge profile (from CV) showed the absence of any active parasitic charge below the buffer layer. R_{sh} values from TLM measurements matched closely with Hall measurements. RT μ_{FE} measured on FatFET structures (L_G ~110um, L_{GS}/L_{GD} ~ 1um) showed peak values of 158 and 168 cm^2/Vs in the doped region for electron densities of 3.5×10^{17} cm^{-3} and 2.1×10^{17} cm^{-3} respectively, which are also the highest values to be ever reported. MOSFETs and MESFETs with device dimensions L_{GS}/L_G/L_{GD} = 1/2.5/5 um show max ON currents of ~200 mA/mm and ~130 mA/mm respectively. MESFETs show very high I_{ON}/I_{OFF} ~ 10^{10} and ultra-low reverse leakage. OFF-state voltage blocking capabilities of these devices will be reported.

These buffer-engineered doped high-mobility Ga_2O_3 channel layers with superior transport properties show great promise for Ga_2O_3 power devices with enhanced performance.

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