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Electronic Transport and Breakdown Phenomena
Room Jefferson 1 & Atrium - Session ET-MoP

ET-MoP-1 Improved Breakdown Voltage and Electrical Characteristics of SrTiO$_3$ Dielectrics on $\beta$-Ga$_2$O$_3$ Power Device, Teakjib Choi, H. Lee, Y. Rim, Sejong University, Korea (Republic of)

High-efficiency semiconductor power switching devices are strongly demanded by society because they can directly contribute to energy conservation and reduction of greenhouse gas emissions around the world. Si-based technologies have been mainstream in communications and digital signal processing as well as power electronics. However, it is recognized that Si powered devices have a limitation of the theoretical performance in terms of material properties. Gallium oxide (Ga$_2$O$_3$) is an emerging wide band gap semiconductor for high power, low loss transistors and diodes due to its excellent material properties and suitability for mass production. The growing interest in metal oxide semiconductor field effect transistors (MOSFETs) for high efficiency power and RF switching has required high dielectric/Ga$_2$O$_3$ interface quality to minimize off-state gate leakage and achieve optimal on-state performance. In this work, we present SrTiO$_3$ thin film as higher-K dielectrics by using pulsed laser deposition process strategies developed and optimized to achieve both high breakdown voltage and low leakage currents at the same time. Therefore, with advances in manufacturing, new strategies and techniques for characterization are also discussed for achievement of novel power devices.

ET-MoP-2 Electric Field Mapping in $\beta$-Ga$_2$O$_3$ by Photocurrent Spectroscopy, Darpan Verma, M. Adnan, S. Dhara, Ohio State University; C. Sturm, Universitat Leipzig, Germany; S. Rajan, R. Myers, Ohio State University

Power electronics devices suffer from unexpected field non-uniformity, and high field often degrades these devices by limiting their lifetime. Electric-field mapping could aid in the design of device features non-destructively by identifying breakdown regions. We will discuss progress in developing an E-field mapping technique that can spatially map out the E-field maxima in $\beta$-Ga$_2$O$_3$ space charge regions and could identify E-field hotspots at which the breakdown is likely. Previously, we showed that the Exciton Franz-Keldysh (XFK) effect can be used to estimate the local E-field maximum in (010) $\beta$-Ga$_2$O$_3$ Schottky diodes based on the redshift of the photocurrent spectral peak.$^1$ In that study, we implemented an XFK model using an analytical approximation for the XFK effect based on the modified Wannier-Mott model. Here, we extend these measurements to higher photon energies ($\geq 5.6$ eV) in (001) $\beta$-Ga$_2$O$_3$ Schottky diodes, and observe a total of three absorption peaks whose intensity varies with the angle of the linear polarization of the monochromatic UV light incident on the device. The three peaks at 4.9 eV, 5.2 eV and at 5.5 eV, match quasi-particle-OFT transitions as well as measurements in $\beta$-Ga$_2$O$_3$ from previous studies.$^2$ Peaks at 4.9 eV and 5.2 eV correspond to excitons polarized within the a-c plane, and the peak at 5.5 eV corresponds to excitons along the b axes. These peaks red shift with bias and can be calibrated to serve as an E-field sensors. A well-calibrated vertical Schottky barrier diode was fabricated on a 10um thick HVPE grown (001) $\beta$-Ga$_2$O$_3$ epitaxial layer ($N_D=1.5E16$/cm$^2$). For the top Schottky contact, a circular Pt (5nm) layer was deposited by E-beam evaporation. Further, leaving the center of the Pt layer exposed for light illumination, a circular ring (overlapping the thin Pt layer) with a contact pad was fabricated using Pt/Au (30/70nm). Afterward, an ohmic back contact of Ti/Au (30/70nm) was blanket deposited. At this structure, the parallel-plate electric field can be theoretically estimated to calibrate the redshift of the photocurrent peaks to E-field values and convert the spatially-resolved photocurrent spectra into mapped E-field values across the whole device active region.

References:

ET-MoP-3 Activation of Si, Ge, and Sn Donors in High-Resistivity Halide Vapor Phase Epitaxial $\beta$-Ga$_2$O$_3$N: Joseph Spencer, Naval Research Laboratory/ Virginia Tech CPES; M. Tadger, A. Jacobs, M. Masto, J. Gallagher, J. Freitas, Jr, Naval Research Laboratory; T. Tu, A. Kuramata, K. Sasaki, Novel Crystal, Japan; Y. Zhang, Virginia Tech (CPES); T. Anderson, K. Hobart, Naval Research Laboratory

With an ultra-wide bandgap (4.8eV), high critical field (6-8MV/cm) and melt-growth capability, the popularity of Gallium oxide (GO) has surged within the material growth and electronic device fields. Even with an UWBG, dopants such as Si and Sn have been shown to be shallow donors (30 and 60meV, respectively) [1-2]. It has also been demonstrated that the addition of nitrogen acceptors allows for the UID level to fall as low as 10$^{14}$/cm$^3$, extending the doping range of GO by over an order of magnitude [3,4]. The inclusion of N also results in a highly resistive current blocking layer (CBL) in GO due to the deep acceptor state formed by the N dopants. In this work we demonstrate how implanted donors can overcompensate the highly resistive GO:N CBL, resulting in highly conductive films while the implanted regions remain highly resistive.

Halide vapor phase epitaxial (HVPE) films were grown on semi-insulating (001) GO:Fe substrates. Prior works [5] characterized the films using Secondary ion mass spectrometry (SIMS) to confirm the presence of the N acceptor and 9.2 \textmu m thickness. C-V measurements showed a net free carrier concentration below the detectable limit of 10$^{14}$ cm$^{-3}$ ($N_D-N_A$). Lateral Schottky diodes showed breakdown voltages that surpassed 2KV for the resistive films [5].

Linear/circular transfer length method (LTLM/CTLM) and van der Pauw (VdP) structures were patterned for donor implantation. Si, Ge, and Sn donors were implanted with a box profile of 100nm at a dose of 3.1x10$^{15}$/cm$^2$. Implanted donors were activated with a rapid thermal anneal (RTA) at 925C for 30min in N2. The LTLM/CTLM and VdP structures were isolated using an 800W BCl$_3$ reactive ion etcher for a 150nm etch. Ti/Au ohmic contacts were deposited following by a contact anneal.

A contact resistance ($R_C$) of 1.2 \textOmega mm and 2.3 \textOmega mm for the Si and Sn implanted samples, respectively was measured from LTLM/CTLMs. Temperature dependent Hall effect measurements (15-300K) gave the sheet carrier concentration ($n_s$), sheet resistance ($R_{sh}$), and mobility ($\mu$). Hall structures that did not receive implantation of the active region between the ohmic contacts could not be measured due to excessive resistance demonstrating retention of N doped film resistivity. Full implanted VdP structures were highly conductive and measurable. At 300K, the Si, Ge, and Sn doped samples achieved mobilities, sheet resistances, and sheet electron densities of 86, 71, and 59 cm$^2$/Vs, 324, 941, and 1750 $\Omega$/sq, and 2.25x14, 9.3x13, and 6.0x13 cm$^{-2}$ respectively. The implant activation efficiency was found to be 66%, 28%, and 18% for Si, Ge, and Sn, respectively. See supplemental page for references.
Electrical and Photonic Devices, Circuits and Applications
Room Jefferson 2-3 - Session EP-WeM

Moderator: Uttam Singisetti, University of Buffalo, SUNY

9:15am EP-WeM-4 Remarkable Improvement of Conductivity in β-Ga$_2$O$_3$
by High-Temperature Si Ion Implantation, Arka Sarkar, T. Isaac-Smith, S. Dhar, Auburn University; J. Lawson, N. Merrett, Air Force Research Laboratory, USA

Monoclinic Beta Gallium Oxide (β-Ga$_2$O$_3$) is emerging as a promising wide bandgap semiconductor for high voltage electronics. Ion implantation is a key process for device fabrication as it provides a unique way to carry out selective area doping with excellent control. It has been demonstrated that Si implantation into (010) β-Ga$_2$O$_3$ at room temperature followed by annealing at ~1000°C results in an activation efficiency (η) of 63% for Si concentrations up to ~3e19 cm$^{-3}$. However, for higher concentrations, a severe drop of the η to 6% occurs [1]. In this work, we demonstrate that high-temperature implantation can be used to significantly improve this for heavily implanted β-Ga$_2$O$_3$. In the case of SiC, implantation at ~500°C results in superior conductivity due to lower defect densities and better recrystallization after annealing [2]. Based on this, we performed room temperature (RT, 25°C) and high temperature (HT, 600°C) Si implants into MBE grown 300 nm (010) β-Ga$_2$O$_3$ films with energies of 275 keV and 425 keV through ~110 nm Mo and ~30 nm Al$_2$O$_3$ layers; with a total of fluence of 2.4e15 cm$^{-2}$ or 4.8e15 cm$^{-2}$. This was followed by annealing in flowing nitrogen at 970°C for 30 minutes to activate the dopants. SIMS shows the Si profile is ~400 nm deep with an average concentration of ~5.0e15 cm$^{-3}$ for the lower fluence samples, and expected to be ~1.2e20 cm$^{-3}$ for the higher fluence (SIMS ongoing). No significant difference in surface roughnesses were detected by AFM throughout the process. HRXRD shows structural defects after the implantation and partial crystallization recovery upon annealing, where the advantage was in favor of HT implantation. The ratio of the free electron concentration from Hall measurements and the total amount of Si in β-Ga$_2$O$_3$ was used to determine the activation efficiencies. For the lower fluence, the HT sample shows only a ~6% improvement of η over the RT sample. Remarkably, for the higher fluence, while the RT sample was too resistive for measurement, the HT sample had η close to 70%, with a high sheet electron concentration of 3.3e15 cm$^{-2}$ and excellent mobility of 92.8 cm$^2$/Vs at room temperature. These results are highly encouraging for achieving ultra-low resistance heavily doped β-Ga$_2$O$_3$ layers using ion implantation, which will be discussed further in this presentation.

References:


Acknowledgments:

We acknowledge the support of the Department of Physics, Auburn University.

9:30am EP-WeM-5 Towards Lateral and Vertical Ga$_2$O$_3$ Transistors for High Voltage Power Switching, Kornellus Tetzner, J. Würfl, E. Bahat-Treidel, O. Hilt, Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany; Z. Galazka, S. Bin Anooz, A. Popp, Leibniz-Institut für Kristallzüchtung (IKZ), Germany INVITED

Gallium Oxide (Ga$_2$O$_3$) power switching devices are expected to boost efficiency of power converters predominately operating at comparatively high bias voltage levels in the kV range. Thanks to the extraordinarily high energy band gap of 4.9 eV a high device breakdown strength of about 8 MV/cm is expected. Thus it is possible to efficiently utilize these properties for very compact power devices with aggressively minimized gate to drain separation. This enables low resistive on-state and low leakage off-state properties. Most Ga$_2$O$_3$ devices introduced so far rely on volume electron transport properties; only a few 2DEG devices have been demonstrated. In any case the values of electron mobility and saturation velocity in Ga$_2$O$_3$ crystals may depend on crystal orientation and did not yet reach properties being comparable to more developed wide band gap semiconductor families such as GaN and SiC. Nevertheless the benefit of Ga$_2$O$_3$ devices relates to the combination of high breakdown field and electron transport properties and the resulting compact device design strategies are already getting competitive to existing power switching technologies.

The presentation will give an overview on the current status of lateral and vertical Ga$_2$O$_3$ devices with a special emphasis on results obtained at FBH and IKZ [1]. For both cases concepts for epitaxial layer structures and device designs suitable for reaching the targeted performance will be discussed especially in terms of breakdown voltage and channel current density. Critical points for device optimization such as type of gate recess in lateral transistors and concepts of critical electric field reduction in vertical transistors will be addressed.

followed by transition layers to a HT (810°C) Si-doped GaO₃ channel layers (~220 nm) without growth interruption. The (010) Fe-doped GaO₃ substrates were cleaned in HF for 30 mins prior to channel growth. From Hall measurements, this stack design is shown to have an effective RT Hall mobility values in the range 162 – 184 cm²/Vs for doped channel electron densities of 1.5-3.5x10¹⁹ cm⁻³ measured on multiple samples/substrates. These mobility values are higher than the state-of-the-art values in GaO₃ literature. Two types of GaO₃ channel were fabricated in this study: 5x5 mm² diced pieces from 10x15 mm² EFG-grown substrates from NCT, Japan and 2-inch CZ-grown bulk substrates from NG Synoptics, USA. The charge and transport properties were also investigated using CV, TLM, field-effect mobility (μF) measurements and FET current characteristics. Few samples were processed for regrown ohmic contacts to minimize contact resistance. Rd values of 1-2 Ω.mm were achieved. 3D electron densities were verified by CV measurements. Channel charge profile (from CV) showed the absence of any active parasitic charge below the buffer layer. Rd values from TLM measurements matched closely with Hall measurements. RT μF measured on FatFET structures (Lx ~110um, Lx/Ly ~1um) showed peak values of 158 and 168 cm²/Vs in the doped region for electron densities of 3.5x10¹⁹ cm⁻³ and 2.1x10²¹ cm⁻³ respectively, which are also the highest values to be ever reported. MOSFETs and MESFETs with device dimensions Lx/Ly/Lz = 1/2.5/5 μm show max ON currents of >200 mA/mm and ~130 mA/mm respectively. MESFETs show very high high/low ~ 10⁴ and ultra-low reverse leakage. Off-state voltage blocking capabilities of these devices will be reported. These buffer-engineered doped high-mobility GaO₃ channel layers with superior transport properties show great promise for GaO₃ power devices with enhanced performance.

Acknowledgement: This material is based upon work supported by the III-V foundation Block Gift Program 2020-2022. This material is also based upon work supported by the Air Force Office of Scientific Research under award number FA9550-21-0078 (Program Manager: Dr. Ali Sayir). We thank AFRL sensors directorate for discussions.

10:45am EP-WeM-10 6-GaO₃ Lateral FinFETs Formed by Atomic Ga Flux Etching, Ashok Dheenan, N. Kalarickal, Z. Feng, L. Meng, The Ohio State University; A. Fiedler, IKZ Berlin, Germany; C. Joishi, A. Price, J. McGlone, S. Dhara, S. Ringel, H. Zhao, S. Rajan, The Ohio State University 6-GaO₃ is an ultrawide bandgap semiconductor with attractive properties for high-power electronics including a high theoretical breakdown field of 8 MV/cm and availability of melt-grown substrates. Low room-temperature electron mobility and low thermal conductivity result in both high sheet-resistance and high thermal resistance, limiting field-effect transistor performance. A ‘fin’ channel structure can overcome these challenges by utilizing a tri-gate geometry to enable electrostatic control over a high sheet-charge density channel while also providing additional surface area for thermal management in the active region. A key technology process for non-planar devices is low-damage channel growth method. In this work, we demonstrate 6-GaO₃ lateral FinFETs with high sheet charge density fabricated with a novel damage-free atomic Ga flux etching technique [N.K. Kalarickal et al. APL 119 (2021)]. The epitaxial structure was grown by MOVCD on a (010) Fe-doped semi-insulating substrate. An Mg-doped layer was used to compensate Si donors at the substrate-growth interface to eliminate any parasitic channel. A 500 nm buffer layer was used to isolate the 600 nm Si-doped channel from the Mg and Fe dopants. The process flow started with selective-area MOVCD regrowth of n+ source/drain using a PECVD SiO₂ mask patterned by optical lithography and dry etching. Then a SiO₂ mask for the fins and mesa isolation layer was patterned by electron-beam and optical lithography. The sample was etched by atomic Ga flux -in an MBE chamber. Electron-beam evaporated Ti/Au ohmic contacts were annealed in an N₂ ambient. Ni gates were deposited by RF sputtering. Hall measurements revealed a sheet-charge density of 2.28x10¹⁹ cm⁻², a mobility of 134 cm²/Vs and a sheet resistance of 1.77 kΩ/sq. Transfer length method showed a contact resistance of 1.27 Ω.mm, a sheet resistance of 2.03 kΩ/sq and a specific contact resistance of 9.11x10⁻⁶ Ω.cm². C-V measurements at 100 KHz were used to extract a doping density of 6x10¹⁸ cm⁻³ in the channel. Current density is above 250 mA/mm normalised to the total fin width with a device for a gate length of 1.5 μm and an Lx of 2.5 μm. Transfer characteristics show a threshold voltage of 12 V for a fin width of 200 nm. The on/off ratio of 10⁴ is limited by the reverse leakage of the Schottky gate. In summary, 6-GaO₃ FinFETs with scaled fins were fabricated using novel damage-free Ga flux etching and show promising electrical performance. We acknowledge funding from DOE/NNSA under Award Number(s) DE-NA000392 and AFSOR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).

11:00am EP-WeM-11 Insights Into the Behaviour of Leakage Current in Lateral GaO₃ Transistors on Semi-Insulating Substrates, Zequn Chen, A. Mishra, M. Smith, T. Moule, University of Bristol, UK; M. Uren, University of Bristol, UK; S. Kumar, M. Higashiwaki, National Institute of Information and Communications Technology, Japan; M. Kuball, University of Bristol, UK Off-state leakage currents in lateral GaO₃ FET devices have previously been attributed to the presence of unintentional Si (n-type) at the interface between epitaxial grown layer and the substrate [1-4], i.e., a parallel leakage conducting channel. High Fe-doping (>10¹⁸ cm⁻³) at the surface of the GaO₃ substrate, followed by thermal annealing, has been shown to compensate the unintentional Si impurities, thereby reducing the leakage current. However, elevated off-state currents and low on-off ratios have still been observed in these devices [4]. Here, we utilize electrical characterization and TCAD simulations to explore the behaviour of leakage current due to Si impurities at the surface of the substrate in lateral GaO₃ transistors. Lateral GaO₃ transistors studied here were processed on an MBE-grown epitaxial layer on surface-implanted (Fe, p-type) semi-insulating GaO₃ substrates, followed by thermal annealing (more details in ref. 4). The transfer characteristic reveals a pinch-off current (10⁻¹A/mm) with an insensitivity to the gate voltage (Fig 2(a)). The pinch-off current demonstrates ohmic characteristics under opposite drain voltage. The clockwise hysteresis in the C-V and the depletion width (Fig 3) indicate a donor-like trapping effect located near the epitax/substrate interface with an activation energy of 0.5eV determined by drain current transients (Fig 4).

2D TCAD simulations (Fig 5), using the SIMS profile for Fe and Si [4] as input parameters, illustrate that the residual Si at the epitaxy/substrate interface pin the Fermi level near the conduction band, resulting in the formation of a parallel conducting channel at the epitaxy/substrate interface (Fig 5(b)). Electrons, from the traps in the epilayer and the contacts, travel vertically to the parallel channel at that interface under negative gate bias. The insensitivity of the leakage current to the gate voltage can be explained by the pinning of the Fermi level due to the high concentration of residual Si dopants. The leakage current magnitude is mostly governed by the resistance of the UID GaO₃ rather than the parallel conduction channel. The latter is evidenced by the constant resistance of the parallel channel in set of circular isolation structures with different spacing (Fig.6). An activation energy of 0.36eV was determined for the leakage current pathway, which contains contributions from the UID layer and the parallel channel (Fig. 7). The mechanism discussed here highlights the role of residual Si contaminants on leakage current. Reduction in their concentration or full compensation is crucial for enhancing performance and device design respectively.

11:15am EP-WeM-12 Device Figure of Merit Performance of Scaled Gamma-Gate β-GaO₃ MOSFETs, Kyle Liddy, A. Islam, J. Williams, D. Walker, N. Moser, D. Dryden, N. Sepelak, K. Chadak, A. Green, AFRL The dynamic switching loss figure of merit (RₑO₃/β vs. Vₓₑ) is a benchmark used to indicate a device’s potential in power-switching applications. Similarly, the lateral Power Figure of Merit (Rₚₒ₃/βₓ vs. Vₓₑ) indicates a devices conduction losses. This work discusses the fabrication and FOM characterization of optical gate and EBL gate GaO₃ MOSFETs and shows their potential for these application spaces that are currently dominated by other technologies. A 50 nm Si doped β-GaO₃ channel layer was homoeopitaxially grown on a Fe doped (010) substrate by ozone molecular beam epitaxy (MBE) targeting 1.0x10¹⁸ cm⁻³ carrier concentration. Device fabrication began with mesa isolation using a high-power BCl₃/Cl₂ ICP etch. Contact to the active layer was achieved with a Ti/Al/Ni/Al metal stack deposited by electron beam metal evaporation followed by a 470 °C anneal in N₂ ambient for 2 minutes. 20 nm of AlₓO₃ gate dielectric was deposited via plasma-enhanced atomic layer deposition. Optical I-gate contacts were defined on half of the sample via optical stepper lithography followed by Ni/Al metal evaporation. Scaled gamma-gates were defined on the remaining half via electron-beam lithography followed by Ni/Al metal evaporation. Interconnect metal was defined via step-on-step lithography followed by Ti/Al metal evaporation. Gateway capacitance was collected as a function of gate voltage at a frequency of 1 MHz, and can be seen for the various device types in Figures 2 A and B. Integration over the collected gate voltage range produces the experimentally extracted Qₓₑ of 0.0014/0.0011 and 0.00028/0.00078 nC for the
optical and e-beam gate devices respectively. $Q_{GD}$ is calculated assuming maximum depletion of the entire $L_{GD}$. Using the equation $Q = qN_oAT$. This provides a conservative representation of the total gate charge for these devices when $Q_o = Q_{GD} + Q_{OD}$ of .0060/.0041 nC and .0050/.0034 nC for optical and EBL gate devices respectively. Standard DC I-V device characterization was performed and is shown in Figure 3(A-F).
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