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Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 1 & Atrium - Session EP-MoP


Power electronics that can accurately and dependably function at high power densities, high temperatures, and in other extreme conditions are needed to improve efficiency in industrial operations, as well as ensure grid resilience and security. Gallium oxide is an attractive candidate material for such use cases, due to its high figures of merit compared to SiC, GaN, and other industry standards. Traditionally, low-temperature operation requires metal contacts that minimize resistivity at all levels; durability and sustained operation is not the primary focus. As such, the most common metallization strategy utilizes a thin adhesive layer of titanium, capped with a thicker layer of gold. These methods, combined with surface modification techniques have achieved remarkably low contact resistances. Transitioning from low-temperature operation to higher temperature operation requires rethinking contact design, however, as both Ohmic and Schottky contacts can rapidly degrade due to increased thermodynamic and kinetic stressors. Thermodynamic analysis shows that metallic titanium will spontaneously react with Ga2O3 to form an oxide; while this process is kinetically hindered at room temperature, oxidation rapidly increases with increasing temperature leading to rapid degradation at temperatures as low as 200-300 °C. As demonstrated independently by many groups, several related kinetic phenomena can further contribute to contact deterioration including Ti nanocrystal formation and Ti migration to the outermost surface.

Here, we investigate several solutions to this fundamental problem. First, we explore the use of a thinner Ti adhesion layer that is designed to fully react with the Ga2O3 substrate. We hypothesize that this strategy could lead to a thermodynamically stable and conductive TiOx suboxide contact layer and circumvent the problem of Ti diffusion through the Au capping layer. While this strategy results in initial contact resistances comparable to other literature values, we see an overall increase in series resistance during high-temperature (300 °C) operation, suggesting that the deployment of thinner layers of Ti does not ensure adequate high-temperature stability. We hypothesize that morphological changes and/or phase change may be responsible for the high-T instability. Future characterization is underway to elucidate the mechanism of deterioration at higher temperature. As an alternative to Ti we then explore the use of an indium tin oxide (ITO) contact layer, in conjunction with both Pt and Au metallizations, with the goal of low contact/series resistances that are also stable during long-term device operation at 300 °C.

EP-MoP-2 Gate Effects of Channel and Sheet Resistance in β-Ga2O3 Field-Effect Transistors using the TLM Method, Ory Mainon, Department of Electrical Engineering, George Mason University; N. Moser, Air Force Research Laboratory, Sensors Directorate; K. Liddy, A. Green, K. Chabak, Air Force Research Laboratory, Sensors Directorate, USA; C. Richter, K. Cheung, P. Poopkanratana, Nanoscale Device and Characterization Division, National Institute of Standards and Technology; Q. Li, Department of Electrical Engineering, George Mason University

Beta Gallium Oxide (β-Ga2O3) is a rapidly developing semiconductor for high power electronic devices with promising advantages. Accurate characterization of the resistances in β-Ga2O3 field-effect transistors (FETs) are critical to understand and model these devices. Here, we report on extracting contact, channel, and sheet resistances from planar, depletion-mode β-Ga2O3 FETs using the transfer length method (TLM). The results are analyzed in comparison with conventional TLM structures fabricated on the same wafer. The β-Ga2O3 FETs are composed of a 50-nm Si-doped epitaxial layer with a target concentration of 2.4 x 10^{20} cm^{-2} fabricated on a (010) semi-insulating β-Ga2O3 substrate. Aluminum oxide (Al2O3, 20 nm) was used as the gate dielectric and the gate length (Lg) remained constant at 1.94 μm, while the source-drain spacing (Lsd) varied as 3μm, 8 μm, and 13 μm. No back contact was used due to the semi-insulating substrate. Transfer characteristic measurements were taken at room temperature and low drain-source voltage (Vds) of 0.01 V to suppress drain effects on the threshold voltage (Vth), about -4V, for devices at different Lsd spacing. When compared to the TLM structures, we observe a decrease in extracted sheet resistance (Rs), and channel sheet resistance (Rsh) as the channel turns on with increasing gate-source voltage (Vgs). The contact resistance (Rc) is assumed to be constant, and is found to be 27.7 Ω mm at a Vds of 0 V. From a Vgs of -3 V to 3 V (off to on state), Rc quickly decreases from 90.4 kΩ sq^{-1} and appears to plateau at 28.2 kΩ sq^{-1}. We saw a similar trend for Rsh, which decreased from 288 kΩ sq^{-1} to 7.66 kΩ sq^{-1}. From the channel sheet resistance, we can find an accurate field-effect mobility after removing the parasitic resistance. A FET with an Lsd of 3μm was found to have a field-effect mobility of 61 cm^2 V^{-1} s^{-1} at a Vds of 5 V. This work indicates that the channel resistance can be accurately extracted by applying the TLM method to FETs, and further helps understand β-Ga2O3 gate effects on transistor performance.


This work characterizes a lateral β-Ga2O3 Schottky barrier diode (SBD) with an interdigitated contact design fabricated using a homoeopitaxial thin-film. This SBD design can be monolithically integrated into RF power switching circuits with standard lateral FET processing. This technique avoids complex fabrication and losses from heterogeneous integration while maintaining the fast switching capabilities of a thin, lateral channel. Prior literature has shown impressive performance from vertical SBDs [1] and lateral devices on non-native substrates [2], but lateral SBDs on homoepitaxial β-Ga2O3 thin-films are not well explored. To the authors’ knowledge, this is the first demonstration of such a SBD design in β-Ga2O3.

The β-Ga2O3 epitaxial layer is grown by MOCVD with a target thickness of 65 nm. Hall effect measurements indicate Si doping of 3.34x10^17 cm^{-3}, carrier mobility of 86.5 cm^2/V-s, and a sheet resistance of 33.15 kΩ/sq. A surface RMS roughness of 0.839 nm is measured by AFM. Mesa isolation is achieved with a BC11 ICP etch. Ohmic contacts are formed by Si ion implantation and a metal stack of Ti/Al/Ni/Au (25/120/50/50 nm) annealed at 470°C. Implant carrier concentration is measured at 5.976x10^{19} cm^{-3}. Evaporated Pt/Al (20/380 nm) forms the Schottky contact. The first passivation layer is 30 nm of Al2O3 deposited by ALD patterned with BOE. Next, a metal interconnect layer of Ir/Au (10/380 nm) is deposited. Final passivation is ~85 nm of Al2O3 by ALD patterned with a CsF RIE etch. All metal is patterned by photoresist lift off.

The diode features four 4x50 μm anode fingers interdigitated with five 8x50 μm cathode fingers. The anode-cathode spacing is 5 μm. The Pt-Ga2O3 barrier height is extracted from temperature dependent J-V measurements to be 1.742 eV. Fitting to forward bias J-V measurements shows an ideality factor of 2.246 and a build-in voltage of 1.963 V. The diode has a breakdown voltage (Vbd) of 784 V and a specific on-resistance (Ron-s) of 9.132 Ω-cm², normalized to the current carrying region between contacts. This yields a power figure of merit (PFOM) of 67.3 MW/cm². We attribute the poor ideality to the highly resistive epitaxy and the degraded interface caused by the relatively rough surface. This device is competitive with published lateral SBD results, and establishes a baseline to enable further development of β-Ga2O3 RF power switching circuits with a streamlined, monolithic fabrication process.


Implantation of β-Ga2O3 will be critical for low resistance contacts and advanced device structures. Literature suggests good activation of Si implants after annealing under N2, but reversible deactivation of carriers under O2-rich annealing. However, there have been no significant studies establishing annealing behavior as a function of time, temperature, and controlled gas atmospheres. Unintentionally doped (UID) β-Ga2O3 films, grown by plasma assisted molecular beam epitaxy on Fe-doped semi-insulating β-Ga2O3 substrates with a UID thickness >400 nm, were ion implanted with Si to a total dose of 7x10^{14} cm^{-2} at three energies (15-115 keV) through an SiO2 cap (20 nm) to yield a 100 nm box profile with a concentration of

Monday Evening, August 8, 2022
Secondary ion mass spectrometry (SIMS) was used to compare implant profiles to SRIM simulated ion ranges, and to quantify Si diffusion during annealing. A wide range of annealing conditions were studied using a load-locked ultrahigh vacuum compatible quartz tube furnace with precise gas control. Anneal times were varied from 10 to 120 minutes, temperatures from 850 to 1000 °C, and the anneal ambient gas was varied by mixing research plus (RP) N₂ with ultra-high purity (UHP) O₂ to control the oxygen partial pressure (pO₂) between <10⁻⁶ and 1.0 bar. Gases were also selectively passed over a desiccant to reduce the water vapor partial pressure to <10⁻⁸ bar. Sheet resistance, carrier activation, and mobility were determined using van der Pauw structures. Annealing in extremely low pO₂ (forming gas 4% H₂/N₂) resulted in decomposition of the Ga₂O₃, while annealing at pO₂ above 10⁻² bar resulted in minimal carrier activation. Within the moderate pO₂ range, minimizing the partial pressure of water vapor was shown to be critical to achieve high carrier activation, with the negative impact of water vapor becoming more significant with increasing pO₂. Data, however, suggests that a trace level of water vapor may slightly improve carrier activation. Short duration anneals resulted in higher carrier activation with longer times resulting in “over annealing” and reduced carrier density. Optimal anneal temperatures were determined to be between 900 and 950 °C, with lower temperatures showing reduced mobility and higher temperatures exhibiting reduced carrier activation and increased Si diffusion. The optimized anneal conditions for this implant were found to be at 950 °C for 20 minutes under dried RP N₂, with an extended gas purge of the furnace prior to the anneal to remove any residual water vapor, resulting in 88% carrier activation and a mobility of 72 cm²/V-s (Rₛ = 130 Ω/sq).
Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 2-3 - Session EP-WeM

Process & Devices III
Moderator: Uttam Singisetti, University of Buffalo, SUNY

9:15am EP-WeM-4 Remarkable Improvement of Conductivity in B-Ga2O3 by High-Temperature Si Ion Implantation, Arka Sardar, T. Issaacs-Smith, S. Dhur, Auburn University; J. Lawson, N. Merrett, Air Force Research Laboratory, USA

Monoclinic Beta Gallium Oxide (β-Ga2O3) is emerging as a promising wide bandgap semiconductor for high voltage electronics. Ion implantation is a key process for device fabrication as it provides a unique way to carry out selective area doping with excellent control. It has been demonstrated that Si implantation into (010) β-Ga2O3 at room temperature followed by annealing at ~1000°C results in an activation efficiency (η)of 63% for Si concentrations up to ~5e19 cm⁻³. However, for higher concentrations, a severe drop of the η to 6% occurs [1]. In this work, we demonstrate that high-temperature implantation can be used to significantly improve this for heavily implanted β-Ga2O3. In the case of SiC, implantation at ~50°C results in superior conductivity due to lower defect densities and better recrystallization after annealing [2]. Based on this, we performed room temperature (RT, 25°C) and high temperature (HT, 600°C) Si implants into MBE grown 300 nm (010) β-Ga2O3 films with energies of 275 keV and 425 keV through ~110 nm Mo and ~30 nm Al2O3 layers; with a total of fluence of 2.4e15 cm⁻² or 4.8e15 cm⁻². This was followed by annealing in flowing nitrogen at 970°C for 30 minutes to activate the dopants. SIMS shows the Si profile is ~400 nm deep with an average concentration of ~6.0e19 cm⁻³ for the lower fluence samples, and expected to be ~1.2e20 cm⁻³ for the higher fluence (SIMS ongoing). No significant difference in surface roughnesses were detected by AFM throughout the process. HRXRD shows structural defects after the implantation and partial crystallization recovery upon annealing, where the advantage was in favor of HT implantation. The ratio of the free electron concentration from Hall measurements and the total amount of Si in β-Ga2O3 was used to determine the activation efficiencies. For the lower fluence, the HT sample shows only a ~6% improvement of η over the RT sample. Remarkably, for the higher fluence, while the RT sample was too resistive for measurement, the HT sample had η close to 70%, with a high sheet electron concentration of 3.3e15 cm⁻² and excellent mobility of 92.8 cm²/Vs at room temperature. These results are highly encouraging for achieving ultra-low resistance heavily doped β-Ga2O3 layers using ion implantation, which will be discussed further in this presentation.

References:

Acknowledgments:
We acknowledge the support of the Department of Physics, Auburn University.

9:30am EP-WeM-5 Towards Lateral and Vertical Ga2O3 Transistors for High Voltage Power Switching, Kornellius Tetzner, J. Würfl, E. Bahat-Treidel, O. Hilt, Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany; Z. Galazka, S. Bin Anooz, A. Popp, Leibniz-Institut für Kristallzüchtung (IKZ), Germany

Invited Gallium Oxide (Ga2O3) power switching devices are expected to boost efficiency of power converters predominately operating at comparatively high bias voltage levels in the kV range. Thanks to the extraordinarily high energy band gap of 4.9 eV a high device breakdown strength of about 8 MV/cm is expected. Thus it is possible to efficiently utilize these devices for very compact power devices with aggressively minimized gate to drain separation. This enables low resistive on-state and low leakage off-state properties. Most Ga2O3 devices introduced so far rely on volume electron transport properties; only a few 2DEG devices have been demonstrated. In any case the values of electron mobility and saturation velocity in Ga2O3 crystals may depend on crystal orientation and did not yet reach properties being comparable to more developed wide band gap semiconductor families such as GaN and SiC. – Nevertheless the benefit of Ga2O3 devices relates to the combination of high breakdown field and electron transport properties and the resulting compact device design strategies are already getting competitive to existing power switching technologies.

The presentation will give an overview on the current status of lateral and vertical Ga2O3 devices with a special emphasis on results obtained at FBH and IKZ [1]. For both cases concepts for epitaxial layer structures and device designs suitable for reaching the targeted performance will be discussed especially in terms of breakdown voltage and channel current density. Critical points for device optimization such as type of gate recess in lateral transistors and concepts of critical electric field reduction in vertical transistors will be addressed.


10:15am EP-WeM-8 Comparison of B-Ga2O3 Mosfets With TiW and NiAl Metal Gates for High-Temperature Operation, Nicholas Sepelak, KBR, Wright State University; D. Dryden, KBR, R. Kohler, University of Texas at Dallas; J. Williams, Air Force Research Lab, Sensors Directorate; T. Asel, Air Force Research Laboratory, Materials and Manufacturing Directorate; H. Lee, University of Illinois at Urbana-Champaign; K. Gann, Cornell University; A. Popp, Leibniz-Institut für Kristallzüchtung, Germany; K. Liddy, Air Force Research Lab, Sensors Directorate; K. Leedy, Air Force Research Laboratory, Sensors Directorate; W. Wang, Wright State University; W. Zhu, University of Illinois at Urbana-Champaign; M. Thompson, Cornell University; S. Mou, Air Force Research Laboratory, Materials and Manufacturing Directorate, USA; K. Chabak, A. Green, Air Force Research Laboratory, Sensors Directorate; A. Islam, Air Force Research Laboratory, Sensors Directorate

B-Ga2O3 offers a robust platform for operation of electronic devices at a high temperature because of its large band gap and low intrinsic carrier concentration. We have recently characterized the high temperature performance B-Ga2O3 field effect transistors using different gate metals in vacuum and air ambient at temperatures up to 500 °C.

The devices fabricated using TiW refractory metal gate and Al2O3 gate dielectric exhibited stable operation up to 500 °C in vacuum and up to 450 °C in air [1]. Transfer (I_DSO-V_GSO) characteristics of a device were measured at various temperatures in vacuum and air. Extracted h_eff/Peff for the vacuum test reduced from ~10⁻¹ to 10⁻² as temperature was increased up to 500 °C. During the vacuum characterization, the contact resistance remained unchanged at all temperatures and, therefore, device characteristics showed no degradation once devices were brought back to RT even after several hours of device operation at 500 °C in vacuum.

The devices, fabricated with Ni/Au gate metal and Al2O3 gate dielectric, exhibited stable operation up to 500 °C in air [2]. The measured I DS/ISO characteristics showed no current degradation up to 450 °C. At 500 °C, the device exhibited a drop in I DS; however, device characteristics recovered once the device is brought back to RT, even after 20 hours of device operation at 500 °C.

For tests in air ambient, both Ni/Au and TiW devices observed an increase in current in vacuum due to activation carriers from dopants/traps in the device, however both exhibited I DS/ISO < 10⁻¹ at 450 °C because of contact degradation. The barrier height of φB^φO≈ 1.0 eV and 0.77 eV was calculated for the TiW/Al2O3 and the NiAl/Al2O3 interfaces, respectively using thermionic emission theory. Thought the values of φT for the Ti/W contacts was consistent with that expected from the work-function difference between TiW and Al2O3, the devices with Ni/Au yielded lower φT presumably due to the diffusion of Ni and the partial crystallization of the Al2O3 dielectric [3]. Our results suggest that with appropriate choice of metals and gate dielectrics, the stable 500 °C operation using B-Ga2O3 is achievable.

followed by transition layers to a HT (810°C) Si-doped GaO3 channel layers (~220 nm) without growth interruption. The (010) Fe-doped GaO3 substrates were cleaned in HF for 30 mins prior to channel growth. From Hall measurements, this stack design is shown to have an effective RT Hall mobility values in the range 162 – 184 cm²/Vs for doped channel electron densities of 1.5-3.5x10¹⁸ cm⁻³ measured on multiple samples/substrates. These mobility values are higher than the state-of-the-art values in GaO3 literature. Two types of (010) Fe-doped GaO3 bulk substrates were used in this study: 5x5 mm² diced pieces from 10x15 mm² EFG-grown substrates from NCT, Japan and 2-inch CZ-grown bulk substrates from NG Synoptics, USA.

The charge and transport properties were also measured. CV, TLM, fieldeffect mobility (μe) measurements and FET current characteristics. Few samples were processed for regrown ohmic contacts to minimize contact resistance. Rr values of 1-2.0 mm were achieved. 3D electron densities were verified by CV measurements. Channel charge profile (from CV) showed the absence of any active parasitic charge below the buffer layer. Rr values from TLM measurements matched closely with Hall measurements. RT μe measured on FET/FET structures (Lx = 110um, Lw/Lx ~ 1um) showed peak values of 156 and 168 cm²/Vs in the doped region for electron densities of 3.5x10¹⁸ cm⁻³ and 2.1x10¹⁷ cm⁻³ respectively, which are also the highest values to be ever reported. MOSFETs and MESFETs with device dimensions Lw/Lx/GD = 1.2/5/5/5 μm show max ON currents of ~200 mA/mm and ~130 mA/mm respectively. MESFETs show very high low/low ~ 10² and ultra-low reverse leakage. Offset-state voltage blocking capabilities of these devices will be reported. These buffer-engineered doped high-mobility GaO3 channel layers with superior transport properties show great promise for GaO3 power devices with enhanced performance.

Acknowledgement: This material is based upon work supported by the I-IT foundation Block Gift Program 2020-2022. This material is also based upon work supported by the Air Force Office of Scientific Research under award number FA9550-21-0078 (Program Manager: Dr. Ali Sayir). We thank AFRL sensors directorate for discussions.

Wednesday Morning, August 10, 2022

10:45am EP-WeM-10 6-BaO3 Lateral FinFETs Formed by Atomic Ga Flux Etching, Ashok Dheenan, N. Kalarickal, Z. Feng, L. Meng, The Ohio State University; A. Fiedler, IKZ Berlin, Germany; C. Joishi, A. Price, J. McGlone, S. Dhara, S. Ringel, H. Zhao, S. Rajan, The Ohio State University

6-BaO3 is an ultrawide bandgap semiconductor with attractive properties for high-power electronics including a high theoretical breakdown field of 8 MV/cm and availability of melt-grown substrates. Low room-temperature electron mobility and low thermal conductivity result in both high sheet resistance and high thermal resistance, limiting field-effect transistor performance. A fin channel structure can overcome these challenges by utilizing a tri-gate geometry to enable electrostatic control over a high sheet-charge density channel while also providing additional surface area for thermal management in the active region. A key process technology for non-planar devices is low-damage fin etch method. In this work, we demonstrate 6-BaO3 lateral FinFETs with high sheet charge density fabricated with a novel damage-free atomic Ga flux etching technique (N.K. Kalarickal et al. APL 119 (2021)). The epitaxial structure was grown by MOVCD on a (010) Fe-doped semi-insulating substrate. An Mg-doped layer was used to compensate Si donors at the substrate-growth interface to eliminate any parasitic channel. A 500 nm buffer layer was used to isolate the 600 nm Si-doped channel from the Mg and Fe dopants. The process flow started with selective-area MOVCD regrowth of n+ source/drain using a PECD SiO3 mask patterned by optical lithography and dry etching. Then a SiO mask for the fins and mesa isolation layer was patterned by electron-beam and optical lithography. The sample was etched by atomic Ga flux in an MBE chamber. Electron-beam evaporated Ti/Al ohmic contacts were annealed in an N2 ambient. Nj gates were deposited by RF sputtering. Hall measurements revealed a sheet-charge density of 2.28x10¹⁵ cm⁻², a mobility of 134 cm²/Vs and a sheet resistance of 1.77 kΩ. Transfer length method showed a contact resistance of 1.27 Ω.mm, a sheet resistance of 2.03 kΩ/Vs and a specific contact resistivity of 9.11x10⁻⁵ Ω.cm². CV measurements at 100 KHz were used to extract a doping density of 6x10¹⁵ cm⁻³ in the channel. Current density is above 250 mA/mm normalized to the total fin width for a device with a gate length of 1.5 μm and an Lw of 2.5 μm. Transfer characteristics show a threshold voltage of 12 V for a fin width of 200 nm. The on/off ratio of 10³ is limited by the reverse leakage of the Schottky gate. In summary, 6-BaO3 FinFETs with scaled fins were fabricated using novel damage-free Ga flux etching and show promising electrical performance. We acknowledge funding from DOE/NNSA under Award Number(s) DE-NA000392 and AFSOR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).

11:15am EP-WeM-12 Device Figure of Merit Performance of Scaled Gamma-Gate β-BaO3 MOSFETs, Kyle Liddy, A. Islam, J. Williams, D. Walker, N. Moser, D. Dryden, N. Sepetak, K. Chabak, A. Green, AFRPL

The dynamic switching loss figure of merit (Roff/Vth) is a benchmark used to indicate a device’s potential in power-switching applications. Similarly, the lateral Power figure of Merit (Pmax/VA) indicates a devices conduction losses. This work discusses the fabrication and FOM characterization of optical gate and EBL gate GaO3 MOSFETs and shows their potential for these application spaces that are currently dominated by other technologies. A 50 nm Si doped β-BaO3 channel layer was homoeptaxially grown on a Fe doped (010) substrate by ozone molecular beam epitaxy (MBE) targeting 1.0x10¹⁰ cm⁻² carrier concentration. Device fabrication began with mesa isolation using a high-power BCl3/Cl2 ICP etch. Contact to the active layer was achieved with a Ti/Al/Ni/Au metal stack deposited by electron beam metal evaporation followed by a 470°C anneal in N2 ambient for 2 minutes. 20 nm of Al2O3 gate dielectric was deposited via plasma-enhanced atomic layer deposition. Optical I-gate contacts were defined on half of the sample via optical stepper lithography followed by Ni/Au metal evaporation. Scaled gamma-gates were defined on the remaining half via electron-beam lithography followed by Ni/Au metal evaporation. Interconnect metal was defined via step coverage lithography followed by Ti/Au metal evaporation. Gate capacitance was collected as a function of gate voltage at a frequency of 1 MHz, and can be seen for the various device types in Figures 2A and B. Integration over the collected gate voltage range produces the experimentally extracted Qo of 0.0014/0.0011 and 0.00082/0.00078 nC for the
optical and e-beam gate devices respectively. $Q_{GDS}$ is calculated assuming maximum depletion of the entire $L_{GDS}$. Using the equation $Q = qN_o A T$. This provides a conservative representation of the total gate charge for these devices when $Q_e = Q_{GDS} + Q_{SC}$ of .0060/.0041 nC and .0050/.0034 nC for optical and EBL gate devices respectively. Standard DC I-V device characterization was performed and is shown in Figure 3(A-F).
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