Program Overview

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WeM	EP2-WeM: Process and Devices IV

Electronic and Photonic Devices, Circuits and Applications
Room Jefferson 2-3 - Session EP2-WeM

Process and Devices IV

Moderator: Christina DiMarino, Virginia Tech

10:45am **EP2-WeM-10 *β*-Ga_2O_3 Lateral FinFETs Formed by Atomic Ga Flux Etching**, ***Ashok Dheenan***, *N. Kalarickal, Z. Feng, L. Meng,* The Ohio State University*; A. Fiedler,* IKZ Berlin, Germany*; C. Joishi, A. Price, J. McGlone, S. Dhara, S. Ringel, H. Zhao, S. Rajan,* The Ohio State University

β-Ga_2O_3 is an ultrawide bandgap semiconductor with attractive properties for high-power electronics including a high theoretical breakdown field of 8 MV/cm and availability of melt-grown substrates. Low room-temperature electron mobility and low thermal conductivity result in both high sheet-resistance and high thermal resistance, limiting field-effect transistor performance. A 'fin' channel structure can overcome these challenges by utilizing a tri-gate geometry to enable electrostatic control over a high sheet-charge density channel while also providing additional surface area for thermal management in the active region. A key process technology for non-planar devices is a low-damage etch method. In this work, we demonstrate *β*-Ga_2O_3 lateral FinFETs with high sheet charge density fabricated with a novel damage-free atomic Ga flux etching technique [N.K. Kalarickal *et* al. APL **119** (2021)]. The epitaxial structure was grown by MOCVD on a (010) Fe-doped semi-insulating substrate. An Mg-doped layer was used to compensate Si donors at the substrate-growth interface to eliminate any parasitic channel. A 500 nm buffer layer was used to isolate the 600 nm Si-doped channel from the Mg and Fe dopants. The process flow started with selective-area MOCVD regrowth of n+ source/drain using a PECVD SiO_2 mask patterned by optical lithography and dry etching. Then a SiO_2 mask for the fins and mesa isolation layer was patterned by electron-beam and optical lithography. The sample was etched by atomic Ga flux -in an MBE chamber. Electron-beam evaporated Ti/Au ohmic contacts were annealed in an N_2 ambient. Ni gates were deposited by RF sputtering. Hall measurements revealed a sheet-charge density of 2.28×10^{13} cm^{-2}, a mobility of 134 cm^2/V.s and a sheet resistance of 1.77 kΩ/sq. Transfer length method showed a contact resistance of 1.27 Ω.mm, a sheet resistance of 2.03 kΩ/sq and a specific contact resistivity of 9.11×10^{-6} Ω.cm^2. C-V measurements at 100 KHz were used to extract a doping density of 6×10^{17} cm^{-3} in the channel. Current density is above 250 mA/mm normalized to the total fin width for a device with a gate length of 1.5 µm and an L_{SD} of 2.5 µm. Transfer characteristics show a threshold voltage of -12 V for a fin width of 200 nm. The on/off ratio of 10^5 is limited by the reverse leakage of the Schottky gate. In summary, *β*-Ga_2O_3 FinFETs with scaled fins were fabricated using novel damage-free Ga flux etching and show promising electrical performance. We acknowledge funding from DOE/NNSA under Award Number(s) DE-NA000392 and AFOSR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).

11:00am **EP2-WeM-11 Insights Into the Behaviour of Leakage Current in Lateral Ga_2O_3 Transistors on Semi-Insulating Substrates**, *Z. Chen, A. Mishra, M. Smith, T. Moule,* University of Bristol, UK*; M. Uren,* University of Brsitol, UK*; S. Kumar,* ***Masataka Higashiwaki,*** National Institute of Information and Communications Technology, Japan*; M. Kuball,* University of Bristol, UK

Off-state leakage currents in lateral Ga_2O_3 FET devices have previously been attributed to the presence of unintentional Si (n-type) at the interface between epitaxial grown layer and the substrate [1-4], i.e., a parallel leakage conducting channel. High Fe-doping (>10^{19} cm^{-3}) at the surface of the Ga_2O_3 substrate, followed by thermal annealing, has been shown to compensate the unintentional Si impurities, thereby reducing the leakage current. However, elevated off-state currents and low on-off ratios have still been observed in these devices [4]. Here, we utilize electrical characterization and TCAD simulations to explore the behaviour of leakage current due to Si impurities at the surface of the substrate in lateral Ga_2O_3 transistors.

Lateral Ga_2O_3 transistors studied here were processed on an MBE-grown epitaxial layer on surface-implanted (Fe, p-type) semi-insulating Ga_2O_3 substrates, followed by thermal annealing (more details in ref. 4). The transfer characteristic reveals a pinch-off current (10^{-7}A/mm) with an insensitivity to the gate voltage (Fig 2(a)). The pinch-off current demonstrates ohmic characteristics under opposite drain voltage. The clockwise hysteresis in the C-V and the depletion width (Fig 3) indicate a donor-like trapping effect located near the epitaxy/substrate interface with an activation energy of 0.5eV determined by drain current transients (Fig 4).

2D TCAD simulations (Fig 5), using the SIMS profile for Fe and Si [4] as input parameters, illustrate that the residual Si at the epitaxy/substrate interface pin the Fermi level near the conduction band, resulting in the formation of a parallel conducting channel at the epitaxy/substrate interface (Fig 5(b)). Electrons, from the traps in the epilayer and the contacts, travel vertically to the parallel channel at that interface under negative gate bias. The insensitivity of the leakage current to the gate voltage can be explained by the pinning of the Fermi level due to the high concentration of residual Si dopants. The leakage current magnitude is mostly governed by the resistance of the UID Ga_2O_3 rather than the parallel conduction channel. The latter is evidenced by the constant resistance of the parallel channel in set of circular isolation structures with different spacing (Fig.6). An activation energy of 0.36eV was determined for the leakage current pathway, which contains contributions from the UID layer and the parallel channel (Fig. 7). The mechanism discussed here highlights the role of residual Si contaminants on leakage current. Reduction in their concentration or full compensation is crucial for enhancing performance and device design respectively.

11:15am **EP2-WeM-12 Device Figure of Merit Performance of Scaled Gamma-Gate β-Ga_2O_3 MOSFETs**, ***Kyle Liddy***, *A. Islam, J. Williams, D. Walker, N. Moser, D. Dryden, N. Sepelak, K. Chabak, A. Green,* AFRL

The dynamic switching loss figure of merit ($R_{ON}Q_G$ vs. V_{BK}) is a benchmark used to indicate a device's potential in power-switching applications. Similarly, the lateral Power Figure of Merit ($R_{ON,sp}$ vs. V_{BK}) indicates a devices conduction losses.. This work discusses the fabrication and FOM characterization of optical gate and EBL gate Ga_2O_3 MOSFETs and shows their potential for these application spaces that are currently dominated by other technologies.

A 50 nm Si doped β-Ga_2O_3 channel layer was homoepitaxially grown on a Fe doped (010) substrate by ozone molecular beam epitaxy (MBE) targeting 1.0×10^{18} cm^{-3} carrier concentration. Device fabrication began with mesa isolation using a high-power BCl_3/Cl_2 ICP etch. Contact to the active layer was achieved with a Ti/Al/Ni/Au metal stack deposited by electron beam metal evaporation followed by a 470 ºC anneal in N_2 ambient for 2 minutes. 20 nm of Al_2O_3 gate dielectric was deposited via plasma-enhanced atomic layer deposition. Optical I-gate contacts were defined on half of the sample via optical stepper lithography followed by Ni/Au metal evaporation. Scaled gamma-gates were defined on the remaining half via electron-beam lithography followed by Ni/Au metal evaporation. Interconnect metal was defined via stepper lithography followed by Ti/Au metal evaporation.

Gate capacitance was collected as a function of gate voltage at a frequency of 1 MHz, and can be seen for the various device types in Figures 2 A and B. Integration over the collected gate voltage range produces the experimentally extracted Q_{GS} of .0014/.0011 and .00082/.00078 nC for the optical and e-beam gate devices respectively. Q_{GD} is calculated assuming maximum depletion of the entire L_{GD}, Using the equation $Q = qN_DAT$. This provides a conservative representation of the total gate charge for these devices when $Q_G = Q_{GS} + Q_{GD}$ of .0060/.0041 nC and .0050/.0034 nC for optical and EBL gate devices respectively. Standard DC I-V device characterization was performed and is shown in Figure 3(A-F).

11:30am **EP2-WeM-13 Electromigration of Native Point Defects and Breakdown in Ga_2O_3 Vertical Devices**, *M. Haseman, D. Ramdin,* Ohio State University*; W. Li, K. Nomoto, D. Jena, G. Xing,* Cornell University*;* ***Leonard Brillson,*** Ohio State University

Beyond the extensive literature on the properties and applications of β-Ga_2O_3 for high power devices, the effects of strong electric fields on the Ga_2O_3 microstructure and in particular the impact of electrically active native point defects have been relatively unexplored.We used cathodoluminescence (CL) point spectra and hyperspectral imaging to observe the spatial rearrangement of oxygen vacancy and vacancy-related defects in Ga_2O_3 vertical trench devices under strong reverse bias.The low crystal symmetry of β-Ga_2O_3 leads to unequal migration of V_O and H-related defects under applied bias resulting in a preferential accumulation of donor species near trench corners where the applied field is strongest, increasing the electric field locally and likely leading to breakdown of the dielectric region.Point defect redistribution along the biasing direction demonstrate post-*operando* the reduced surface electric field (RESURF) effect modulated by the device geometry.

We used CL point spectra and HSI mapping to demonstrate how point defect related donor species in β-Ga_2O_3 vertical Schottky diodes migrate and redistribute under high reverse electrical bias.The accumulation of donor-related defects at Schottky barrier trench corners increases the local doping density and decreases the Ga_2O_3 depletion width such that the electric field falls across a narrower total insulator region, thereby increasing the field locally in the nanoscale trench corner.The low crystal symmetry of the monoclinic crystal structure results in unequal migration energies for point defects on inequivalent lattice sites and along inequivalent crystallographic directions, suggesting a preferential migration of specific three-fold coordinated oxygen vacancies and/or migration of positively charged hydrogen species, altering the relative intensity of the UV emissions that we observe via spatially resolved CL maps and linecuts.Together with the local electrical field maximum under reverse bias resulting from the fin/trench design, this local doping increase due to defect migration suggests a point-of-failure near the trench corners. More generally, defect migration and local doping changes under extreme electric fields in β-Ga_2O_3 demonstrates the potential impact of nanoscale device geometry in other high-power semiconductor device structures.

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