Program Overview

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Dielectric Interfaces
Room Jefferson 2-3 - Session DI-TuA
Processes & Devices II

Moderator: Hongping Zhao, Ohio State University

3:45pm **DI-TuA-9 Dielectric Integration on (010) β-Ga_2O_3: Al_2O_3, SiO_2 Interfaces and their Thermal Stability**, ***Ahmad Islam***, Air Force Research Laboratory*; A. Miesle,* University of Dayton*; M. Dietz,* Wright State University*; K. Leedy, S. Ganguli,* Air Force Research Laboratory*; G. Subramanyam,* University of Dayton*; W. Wang,* Wright State University*; N. Sepelak, D. Dryden,* KBR, Inc.*; T. Asel, A. Neal, S. Mou, S. Tetlak, K. Liddy, A. Green, K. Chabak,* Air Force Research Laboratory

Metal-oxide-semiconductor (MOS) devices made using the newest compound semiconductor β-Ga_2O_3 generally do not exhibit high quality, electronic-grade dielectric integration. These are mainly due to the deposition of dielectrics on low-quality substrates. The device fabrication processes also introduce additional defects within the device. The fabricated devices therefore have > 10^{12} cm^{-2} defect density and show a large hysteresis during the C-V and I-V characterization and a large AC-DC dispersion during pulse characterization. A reduction of hysteresis and dispersion often uses a high temperature process that compromises the gate leakage and the breakdown strength of the dielectric. Dielectrics in β-Ga_2O_3 devices also loses its integrity when devices are subjected to high temperature, extreme environment applications.

Here, we will highlight the general challenge for integrating dielectrics on β-Ga_2O_3, address the associated requirements for obtaining high-quality dielectric and dielectric/β-Ga_2O_3 interface, and present our recent works on the integration of $Al_2O_3$and SiO_2 dielectrics on (010) β-Ga_2O_3 [1]. We will show how surface roughness can play key role in controlling interface defect density in β-Ga_2O_3 MOS capacitors. We will also discuss the role of surface cleanliness (using, for example, piranha treatment), the removal of surface defective layer using HF, and the role of post-deposition annealing in reducing interface defect density [2]. Finally, we will compare the thermal stability of SiO_2 and Al_2O_3deposited on (010) β-Ga_2O_3 substrates [3]. All these considerations will eventually allow electronic-grade integration of dielectrics on β-Ga_2O_3substrates needed to attain high breakdown voltage in power electronics applications and also to attain low AC-DC dispersion and high operating frequency in RF applications.

[1] Islam *et al.*, "Integration challenges for dielectric on β-Ga_2O_3 and their solutions," Proc. of *GOMACTech*, 2022, P31.

[2] Islam *et al.*, "Hysteresis-free MOSCAP made with Al_2O_3/(010)β-Ga_2O_3 interface using a combination of surface cleaning, etching and post-deposition annealing," Proc. of *DRC*, 2021, p. 9467169.

[3] Islam *et al.*, "Thermal stability of ALD-grown SiO_2 and Al_2O_3 on (010) β-Ga_2O_3 substrates," Accepted, *DRC*, 2022.

4:00pm **DI-TuA-10 Deep Etch Field-Terminated β-Ga_2O_3 Schottky Barrier Diodes With 4.2 MV/cm Parallel Plate Field Strength**, ***Sushovan Dhara***, *N. Kalarickala, A. Dheenan, C. Joishi, S. Rajan,* The Ohio State University

β-Ga_2O_3 Schottky barrier diodes (SBDs) [1-2] are promising devices for next-generation kV-class power switching. In this work, we analyze the effect of BCl_3/Cl_2 based dry etch on [100] and [010] etched vertical sidewalls and demonstrate a deep mesa etch design for efficient edge termination leading to parallel plate fields in excess of 4 MV/cm. We also report on significant depletion of the semiconductor to depths up to several 10's of micron, and remarkable anisotropy in this depletion. The work demonstrated here provides insight into the impact of etching on n-type Ga_2O_3, and shows a promising method to realize efficient field termination for high breakdown field strength SBDs.

Experimental: The SBDs reported here were fabricated on commercially available (001) n-doped β-Ga_2O_3 layers grown by halide vapor phase epitaxy (HVPE). To analyze etch damage in the etched vertical sidewall planes ([010], [100]), rectangular SBD patterns with varying lengths along (100) and (010) directions were designed and etched (~ 4 µm) in ICP-RIE using BCl_3/Cl_2 with the Pt anode metal as the hard mask. Two terminal reverse breakdown showed breakdown voltages of -1150 V (4.23 MV/cm) for the mesa edge terminated devices, whereas the planar devices broke at -530 V (2.87 MV/cm). The removal of material during the etch reduces image charges, and therefore enables very efficient field termination. Analysis of the forward conduction characteristics shows some unusual effects of the plasma exposure creating deep lateral depletion on the order of 10's of microns. Rectangular mesa devices fabricated with the sidewalls as (010) planes were more susceptible to lateral depletion - devices with less than 100 µm spacing between the (010) sidewalls were very resistive. On the other hand, such deep lateral depletion was not seen from the (100) sidewall. We conclude that the plasma exposure of (010) planes leads to the diffusion laterally into the material, creating defects deep inside the material. A possible reason for this could be the diffusion of BCl_3/Cl_2 etch radicals along the (010) direction[3]. This is the first report of the anisotropic and remarkably deep depletion caused by plasma etching in Ga_2O_3. The high parallel plate field (> 4 MV/cm) also suggests that with proper control, deep etching can be a promising way to achieve field termination in Ga_2O_3 SBDs.

We acknowledge funding from DOE / National Nuclear Security Administration under Award Number(s) DE-NA000392, and AFOSR GAME MURI (Award No. FA9550-18-1-0479, project manager Dr. Ali Sayir).

References: [1] W. Li, et al., IEEE EDL,2020. [2] Z. Xia et al., APL,2019. [3] G. Alfieri et al., JAP.,2021.

4:15pm **DI-TuA-11 Demonstration of Low Thermal Resistance in Ga_2O_3 Schottky Diodes by Junction-Side-Cooled Packaging**, ***Boyan Wang***, *M. Xiao, J. Knoll, Y. Qin,* Virginia Polytechnic Institute and State University*; J. Spencer, M. Tadjer,* U.S. Naval Research Laboratory*; C. Buttay,* Univ Lyon, CNRS, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, Ampère, France*; K. Sasaki,* Novel Crystal Technology, Japan*; G. Lu, C. DiMarino, Y. Zhang,* Virginia Polytechnic Institute and State University

Ga_2O_3 is a promising candidate for power electronics and RF applications, whereas a fundamental limitation of Ga_2O_3 is its low thermal conductivity (k_T). This work studies the impact of the packaging process on Ga_2O_3 device characteristics and measures the junction-to-case thermal resistance ($R_{θJC}$) of a 15 A double-side-packaged vertical Ga_2O_3 Schottky barrier diode (SBD) under the bottom-side-cooling and junction-side-cooling schemes.

Fig. 1. shows the schematic and photo of the packaged Ga_2O_3 SBD, device fabrication process [1], and the device structure. 100-nm Ti and 200-nm Ag were deposited on both anode and cathode as the contact layer for silver sintering. Besides serving as an adhesion layer, Ti also functions as a barrier layer to prevent Ag diffusion into Schottky metal in the subsequent sintering process.

Die attach is performed using a pressureless sintering process in air, using a nano-silver paste. The paste is stencil-printed through a 70 µm thick, laser-cut mask. The size of the silver print is increased from 2.5×2.5 mm^2, the size of the mask opening, to about 3×3 mm^2. Once sintered, the assembly is encapsulated in a silicone elastomer for isolation. Fig. 2 summarizes the packaging process.

Fig. 3 shows the forward I-V, reverse C-V and I-V characteristics of the packaged Ga_2O_3 SBD, revealing a turn-on voltage V_{on} of 0.9 V, a forward current of 15 A at 2.15 V, an on/off ratio of 10^{10} extracted at 2 V/0 V, and a breakdown voltage of about 600 V.

Fig. 4 shows the I-V characteristics of the Ga_2O_3 SBD before and after packaging. After packaging, the V_{on} increases, the differential on-resistance reduces, and both forward and reverse leakage current decreases. These shifts are believed to be due to the improvement of the Schottky contact after the 250°C sintering process.

The $R_{θJC}$ measurement is detailed in [2], following the transient dual interface method, i.e., JEDEC 51-14 standard. Fig. 5 shows our $R_{θJC}$ measurement set-up, the bottom- and junction-cooling measurements of the same packaged Ga_2O_3 SBD. Fig. 6 shows a much lower $R_{θJC}$ (0.5 K/W) under junction-side cooling as compared to the $R_{θJC}$ (1.43 K/W) under the bottom-side cooling.

Table I benchmarks the $R_{θJC}$ of our Ga_2O_3 SBDs against commercial 600-V SiC SBDs with a similar current rating and different TO-series packages. The $R_{θJC}$ of our junction-side cooled Ga_2O_3 SBD is lower than that of the commercial SiC SBDs with similar package size and current rating. This shows the low k_T of Ga_2O_3 can be overcome by packaging solutions.

[1] APL, vol. 115, no. 26, p. 263503, 2019.

[2] IEEE EDL, vol. 42, no. 8, pp. 1132-1135, 2021.

4:30pm **DI-TuA-12 High Temperature In-situ MOCVD-grown Al_2O_3 Dielectric on (010) β-Ga_2O_3 with 10 MV/cm Breakdown Field**, ***Saurav Roy,*** University of California Santa Barbara*; A. Bhattacharyya,* University of Utah*; C. Peterson, S. Krishnamoorthy,* University of California Santa Barbara

We report on the growth and characterization of in-situ Al_2O_3 on (010) β-Ga_2O_3 using metalorganic chemical vapor deposition (MOCVD). The in-situ Al_2O_3 deposition provides an in-situ passivation to the underlying epitaxial β-Ga_2O_3 layer and protects the semiconductor surface from undesired contaminants. The MOCVD growth of Al_2O_3 also facilitates high temperature dielectric deposition compared other conventional techniques, which is known to enhance the bulk and interface quality of the dielectric. The growth of β-Ga_2O_3 was performed in an Agnitron MOVPE reactor with far injection showerhead design using Triethylgallium and Oxygen as precursor gas at a growth temperature of 600 ^{0}C, which is followed by the growth of Al_2O_3 layer at the growth temperature of 810 ^{0}C inside the same chamber using Trimethylaluminum and O_2 as precursors without breaking the vacuum. Thickness of the grown Al_2O_3 layer was extracted to be 23 nm using Xray reflectivity measurements. Using capacitance voltage (CV) measurements, the dielectric constant of the Al_2O_3 layer was extracted to be ~8. The fast and slow near interface traps at the in-situ Al_2O_3/ β-Ga_2O_3 interface were characterized using stressed CV measurements on metal oxide semiconductor capacitor (MOSCAP) structures. The sheet density of near interface trap states with fast and slow emission times were also calculated to be 8.3 x 10^{11} cm^{-2} and 1.5 x 10^{11} cm^{-2} respectively. The density of the interface states (initially filled and unfilled) and bulk oxide hole traps (D_t) and their energy dependences were calculated to be 5.4 x 10^{11} cm^{-2} eV^{-1} using deep ultra-violet assisted CV technique, which is significantly lower than the ALD Al_2O_3/β-Ga_2O_3 interface from literature. Furthermore, the breakdown voltage and leakage currents for the in-situ Al_2O_3/β-Ga_2O_3 MOSCAPs were evaluated using forward and reverse IV characteristics. In the accumulation regime with forward bias, the entire electric field drops across the oxide layer. An average peak breakdown field of approximately 10.2 to 10.6 MV/cm underneath the center of the anode is evaluated. High breakdown field in combination with a dielectric constant close to β-Ga_2O_3, makes this an excellent dielectric/semiconductor platform for high performance device applications. This approach of in-situ dielectric deposition on β-Ga_2O_3 can pave the way as gate dielectrics for future β-Ga_2O_3 based high performance MOSFETs due to its promise of improved interface and bulk quality compared to other conventional dielectric deposition techniques. We acknowledge funding from AFOSR MURI program under Award No. FA9550-21-0078 (PM: Dr. Ali Sayir).

4:45pm **DI-TuA-13 Metal Oxide (PtOX) Schottky Contact with High-k Dielectric Field Plate for Improved Field Management in Vertical β-Ga2O3 Devices**, ***Esmat Farzana,*** University of California Santa Barbara*; A. Bhattacharyya,* The University of Utah*; T. Itoh, S. Krishnamoorthy, J. Speck,* University of California Santa Barbara

β-Ga_2O_3 has emerged interest in high-power electronics due to its high breakdown field (8 MV/cm) and melt-grown substrates. To extract the full potential of β-Ga_2O_3 devices, high reverse blocking capability and field management are fundamental requirements. However, this is challenging in β-Ga_2O_3 due to absence of its p-type that limits high barrier formation in critical field regions. Hence, to enhance the β-Ga_2O_3 diode performance, it is important to have high Schottky barrier material at surface as well as efficient field-plate dielectric. Toward this goal, we developed metal oxide (PtO_x) Schottky contact with high-κ dielectric (ZrO_2) field plate in vertical β-Ga_2O_3 devices to support high electric field at both surfaces and edges. Vertical field-plate Schottky diodes were fabricated at UCSB with HVPE (001) 10 µm β-Ga_2O_3 epitaxy (doping ~2×10^{16} cm^{-3}). The devices had Ti/Au ohmic and Pt cap/PtO_x Schottky of 100 µm diameter. The PtO_x was formed by reactive sputtering of Pt and oxygen. The field plates were investigated with different lengths, 15 µm and 30 µm, with sputter deposited dielectric ZrO_2 (~215 nm). The ZrO_2 was chosen for its ~1.2 eV conduction band offset with β-Ga_2O_3, breakdown field >3 MV/cm, and dielectric constant of ~23. The PtO_x Schottky properties were first characterized with current-voltage (I-V) and capacitance-voltage (C-V), and compared with that of Pt/β-Ga_2O_3 from the same HVPE β-Ga_2O_3 sample. The PtO_x Schottky had a significantly higher barrier height of ~2.1 eV from both I-V and C-V compared to that of Pt with 1.35 eV (I-V)/ 1.6 eV (C-V). The similar barrier height for PtO_x from I-V and C-V indicates its homogeneous interface. The forward current of the field-plate PtO_x diodes also showed near unity ideality factor (1.17) and on-off ratio of ~10^{11}. The minimum specific on-resistance of the PtO_x diodes was 2.6, 2.36, and 2.3 mΩ-cm^2 for devices without field plate, with field plate lengths of 15 µm, and 30 µm respectively. The reverse breakdown of the diodes was characterized at the Univ. of Utah. A maximum breakdown voltage (V_{br}) of 947 V was obtained with 30 µm field plate whereas the diode with 15µm field plate and without field plate showed V_{br} of 882 V and 520 V, respectively. The consistent increase of V_{br} with field plates indicates their field management efficacy. SILVACO simulation showed a peak electric field of 5.12 MV/cm in β-Ga_2O_3 and 3.5 MV/cm in ZrO_2 at V_{br}~950V. The BFOM (0.4 GW/cm^2) of our diodes is comparable or better than most of the reports. As the ZrO_2 breakdown limited to reach the full potential of β-Ga_2O_3, future work will include high breakdown dielectric to further improve the device performance.

5:00pm **DI-TuA-14 Field Plated β-Ga_2O_3 Mis Diodes with High-κ Tio_2 Interlayer for Increased Breakdown and Reduced Leakage Current**, ***Nolan Hendricks,*** Air Force Research Laboratory; UC Santa Barbara*; A. Green, A. Islam, K. Leedy, K. liddy, J. Williams,* Air Force Research Lab*; E. Farzana, J. Speck,* UC Santa Barbara*; K. Chabak,* Air Force Research Lab

β-Ga_2O_3 (BGO) is an ultra-wide bandgap (~4.8 eV) semiconductor with disruptive potential for power electronics due to its predicted breakdown field of 8 MV/cm, ease of n-type doping, and availability of melt-grown native substrates. With no p-type doping, Schottky barriers are essential to limit reverse leakage current in rectifying BGO devices. However, reverse leakage current due to thermionic field emission in such devices exceeds the practical limit of 1 mA/cm^2 at surface fields ($\mathcal{E}_{surf}$) <5 MV/cm for barrier heights <2.2 eV, limiting the potential benefits of BGO. It is desirable to find a solution for reducing leakage current in diodes without efficiency losses from increased turn-on voltage (V_{on}) or specific on-resistance ($R_{on,sp}$). TiO_2 is a high κ (~60) dielectric with a conduction band edge ~0.3 eV *lower* than BGO, presenting the potential for use in metal-interlayer (MIS) diodes to provide a wider tunneling barrier with no increased barrier height for forward conduction.

Pt/TiO_2/β-Ga_2O_3 MIS diodes and Schottky barrier diodes (SBDs) with and without field plates were fabricated on ~5 µm, 6x10^{16} cm^{-3} (001) HVPE BGO on an n+ BGO substrate. A back side Ti/Au contact was RTA annealed at 470 °C for 60 s in N_2 ambient. TiO_2 (4.5 nm) was deposited by atomic layer deposition and removed with BOE in areas for SBDs. Pt/Au anode contacts were deposited, followed by 200 nm PECVD SiO_2 and Ti/Au field plate metal with 20 µm overhang.

Forward current-voltage (I-V) behavior was measured for all device types. An ideality factor of 1.08 and 1.09 was fitted for SBDs and MIS diodes respectively. The minimum differential $R_{on,sp-}$ was ≤1.2 mΩ·cm^2 in all devices, and V_{on} extrapolated from the linear I-V was similar between the SBDs and MIS diodes at 1.4 V.

The leakage current and breakdown of the devices were measured under reverse bias. The SBDs experienced catastrophic breakdown at 453 V (no FP) and 495 V (FP), and both reached 1 mA/cm^2 leakage current at 235 V, corresponding to an $\mathcal{E}_{surf}$ of 2.3 MV/cm. The MIS diodes experienced breakdown at 552 V (no FP) and 666 V (FP). 1 mA/cm^2 leakage current was observed at 408 V (no FP) and 574 V (FP), with corresponding $\mathcal{E}_{surf}$ estimated to be 3.0 MV/cm and 3.5 MV/cm respectively. The BFOM of the field plated MIS diode was 370 MW/cm^2 for hard breakdown and 270 MW/cm^2 when limited to 1 mA/cm^2 leakage current, both of which are the best reported in their respective categories for BGO MIS diodes. The substrate resistance is expected to be ~0.9 mΩ·cm^2, so similarly fabricated devices with lower parasitic resistance are expected to achieve a BFOM >1 GW/cm^2 with leakage <1 mA/cm^2.

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