

Suppression of Stacking Fault Expansion in SiC Epitaxial Layers via Substrate Implantation

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Silicon carbide (SiC) devices can fail during operation due to bipolar degradation [1], where carrier injection causes basal plane dislocations (BPDs) to expand into single Shockley stacking faults (SSFs), leading to increased on-state resistance and reverse current leakage [2,3]. Previous studies have demonstrated that proton and helium implantation within the epitaxial layer can effectively suppress stacking fault expansion [4]. However, at very high carrier injection conditions, such as pulsed-power applications, BPDs propagate from the substrate or highly doped layers into the epitaxial drift layer [5]. This study explores an alternative approach for mitigating BPD propagation and SSF expansion by performing implantation into substrates prior to epitaxial growth of the drift layer. This approach offers a pathway toward improved high-power device reliability.

In this work, 200 mm diameter 4H-SiC substrates were subjected to implants with different species (silicon, carbon, and phosphorus) at varying energy (50-200 keV) and doses ($5 \times 10^{14} - 2.5 \times 10^{15} \text{ cm}^{-2}$). Each wafer had 5 implant regions with one region receiving no implant to allow for a direct comparison of the implantation impact on the BPD faulting and SSF expansion. A 10 μm intentionally doped n-type, $\sim 2 \times 10^{16} \text{ cm}^{-2}$, SiC epitaxial layer was deposited on each of the implanted substrates. During the ramp to growth temperature, the H_2 carrier gas was reduced and the pressure was increased to suppress the etching of the implanted SiC substrate.

Ultraviolet photoluminescence (UVPL) was used to image the wafers before and after prolonged (3hr) UV carrier injection stressing at 9 kWcm^{-2} . We observed in several wafers, at such high injection conditions, BPDs from untreated SiC substrates propagate into the epi-layer. However, for the majority of the implant conditions, over a magnitude reduction in SSF densities were seen. The SSF blocking mechanism is likely due to reduction in carrier lifetime caused by implantation as well as potential pinning from the point defects introduced during implant that block SSFs from expanding into the epitaxial layer. The various defect mechanisms along with complete statistical analysis will be presented.

- [1] P. Bergman et al., Mat. Sci. Forum, **353–356** (2001) 299.
- [2] A. Galeckas et al., Appl. Phys. Lett., **81** (5) (2002) 883.
- [3] Agarwal et. al., IEEE Electron Device Lett., **28** (2007) 587.
- [4] M. Kato et al., Sci Rep, **12** (1) (2022) 18790.
- [5] N. A. Mahadik et al., Appl. Phys. Lett., **100** (4) (2012) 042102.

Table I. Implantation split on 150 mm 4H-SiC wafers

Wafer	Region	Species	Energy (keV)	Dose (cm ⁻²)	SSF Density (cm ⁻²)
1	1	Silicon	200	1.00E+15	60
1	2	Silicon	100	1.00E+15	NA
1	3	Silicon	100	5.00E+14	1
1	4	Silicon	50	5.00E+14	6
1	5	NA	NA	NA	90
2	1	Phosphorus	100	1.00E+15	3
2	2	Phosphorus	200	1.00E+15	NA
2	3	Carbon	100	1.00E+15	0
2	4	Carbon	50	2.50E+15	6
2	5	NA	NA	NA	83

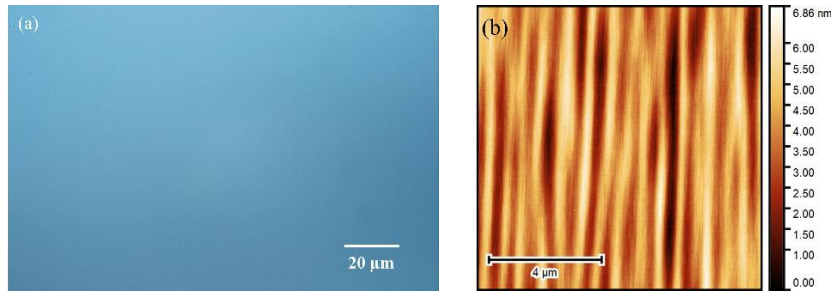


Fig. 1 (a) Nomarski image of representative surface morphology for regions 2-5 and (b) AFM micrograph from region 3 of Wafer 1. Surface roughness is 0.7 nm RMS.

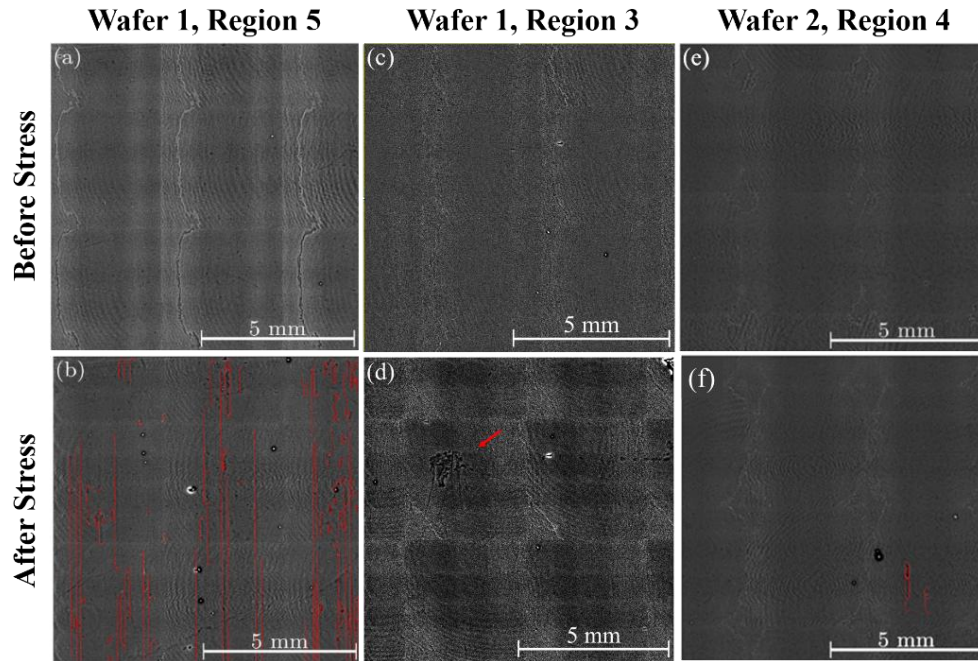


Fig. 1. UVPL images of region 5 and 3 of wafer 1 before (a, c) and after (b, d), and of region 4 of wafer 2 before (e) and after (f) UV stressing. Implantation in region 3 of wafer 1 and region 4 of wafer 2 prevented more SSFs (shown in red) from expanding (d) than in region 5 without implantation (b).