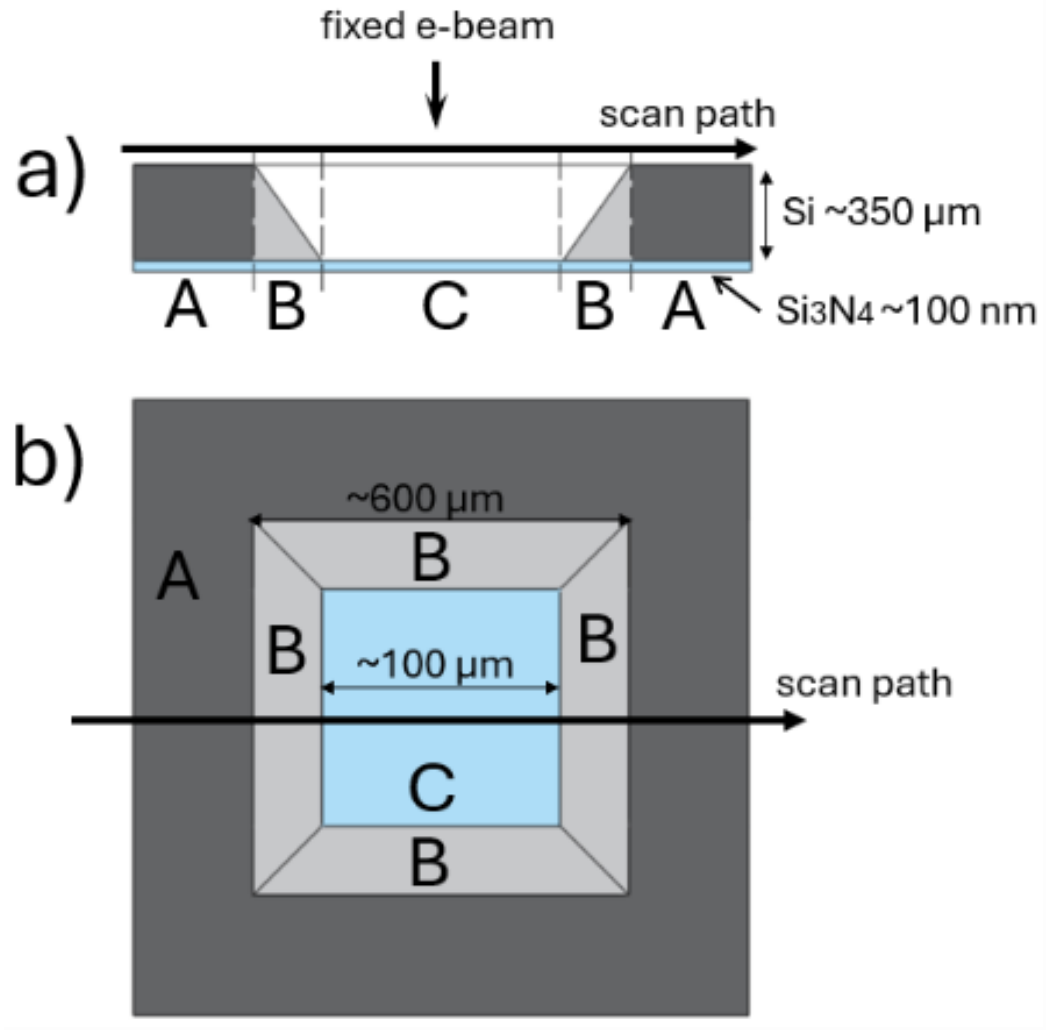

Fig. 1. Schematic of the line-scan experiment (not to scale). a) Cross-section of the Si_3N_4 membrane chip along the scan direction, showing the KOH-etched pyramid cavity, the thin Si_3N_4 membrane spanning its top, and the surrounding silicon substrate, b) top view of the same chip, with the scan line crossing the central membrane window. The arrows labeled "scan path" indicate the direction of sample stage translation - the electron beam is stationary, while the stage is moved beneath it so that successive regions of the chip pass under the beam. Three regions are encountered along the scan: A (dark grey) - full silicon substrate (~350 µm thick), fully absorbing the beam; B (light grey) - sloped pyramid wall formed during KOH etching, where the silicon thickness gradually decreases from 350 µm down to 0; C (blue) - the exposed Si3N4 membrane (100 nm thick), where the beam passes through to the sensor.