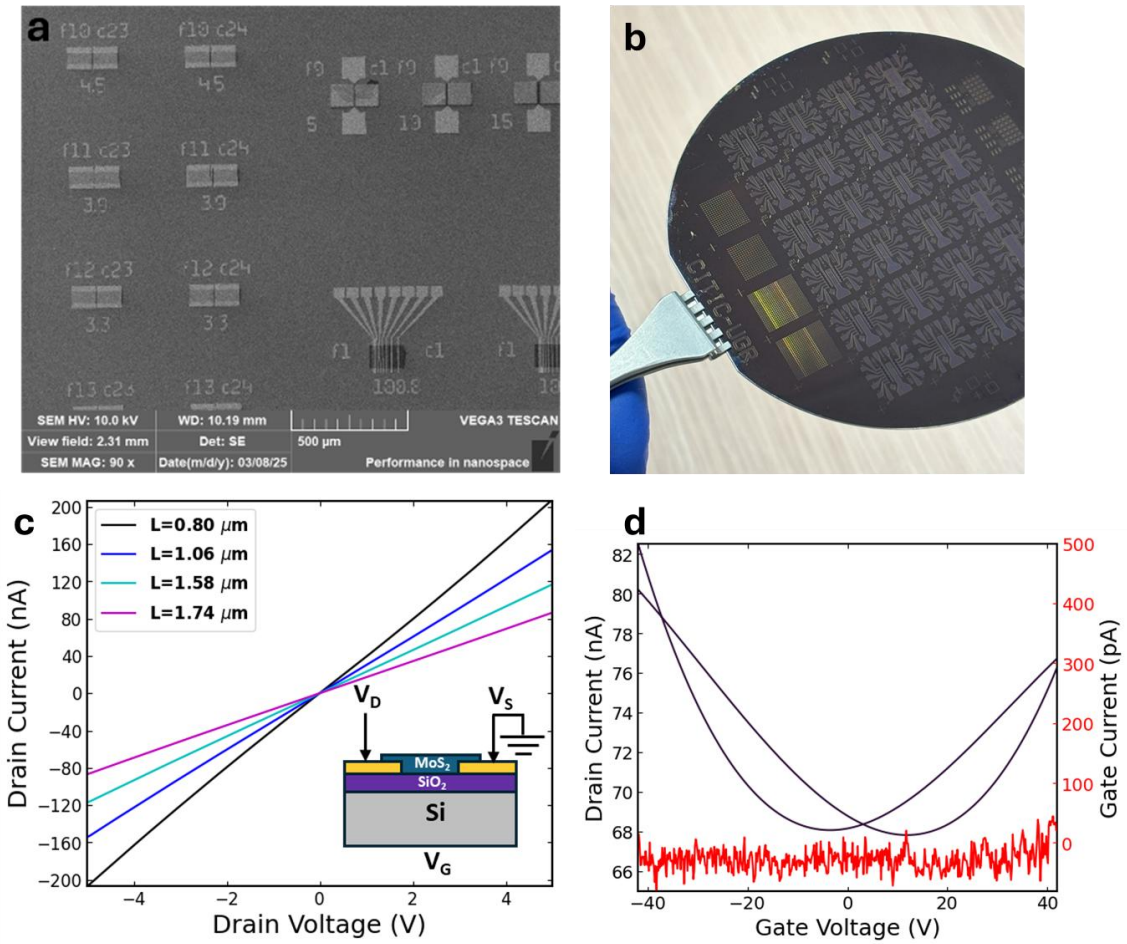

ALD-grown MoS_2 transistor test structures and electrical response.

(a) SEM image of fabricated MoS_2 transistor arrays with different channel geometries used for electrical characterization and resistance extraction. (b) Optical photograph of a processed wafer including multiple device layouts and test structures, highlighting the scalability of the fabrication approach. (c) Output characteristics of back-gated MoS_2 transistors with different channel lengths, showing linear current–voltage behavior and enabling extraction of channel and contact contributions. The inset shows the device cross-section and measurement configuration. (d) Representative back-gate transfer characteristic measured at fixed drain bias, showing weakly polarity-selective/ambipolar behavior of ALD-grown MoS_2 together with low gate leakage current.