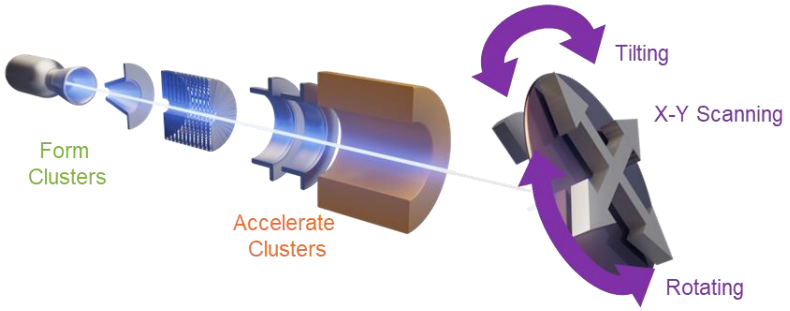


Fig. 1. Schematic of the GCB system. Clusters are generated in a fixed nozzle and then emitted and focused towards the wafer scanner. The scanner is equipped with tilt capability and location specific processing to control the speed of the wafer movement and thus the amount of etching at each location on the wafer

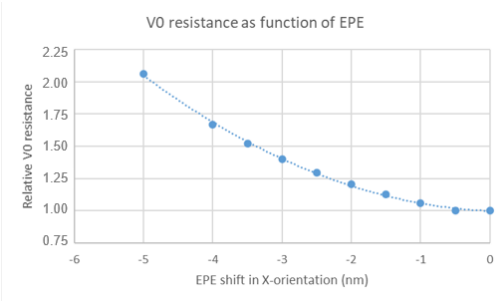


Fig. 2. V0 resistance as a function of EPE. 2.0nm of edge placement error correction can have upwards of 20% improvement in V0 parasitic resistance

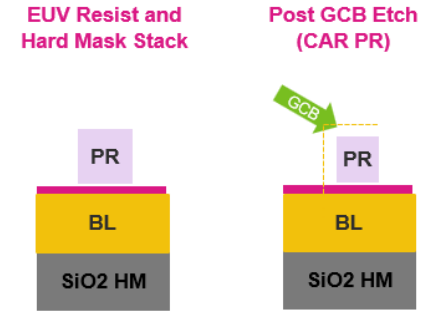


Fig. 3. Schematic of the via lithography stack immediately following EUV lithography exposure and then post GCB etching

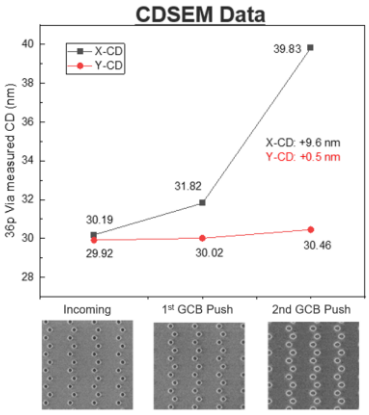
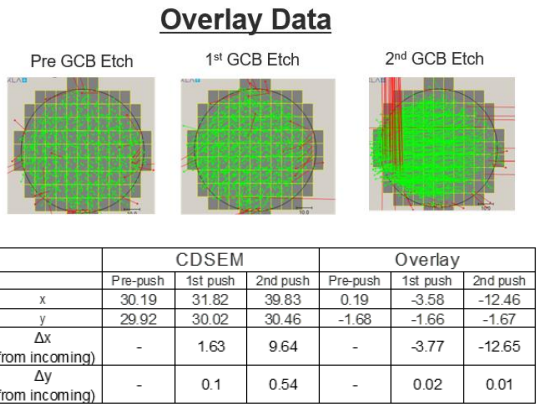


Fig. 4. CDSEM data of a wafer that saw two subsequent GCB etching steps in the X direction. The CD in the X direction grows with each GCB etch while the Y CD stays the same.



	CDSEM			Overlay		
	Pre-push	1st push	2nd push	Pre-push	1st push	2nd push
x	30.19	31.82	39.83	0.19	-3.58	-12.46
y	29.92	30.02	30.46	-1.68	-1.66	-1.67
Δx (from incoming)	-	1.63	9.64	-	-3.77	-12.65
Δy (from incoming)	-	0.1	0.54	-	0.02	0.01

Fig. 5. Overlay maps post lithography and GCB etching. The change in CD in the X direction is similar to the change in measured overlay. The Y CD and overlay values remain essentially unchanged

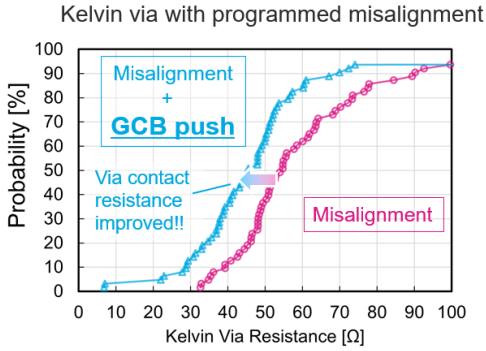


Fig. 6. Kelvin via resistance measurement for two wafers. The wafer that had the misalignment corrected by GCB showed a decrease in the via resistance compared to the misaligned wafer with no adjustment

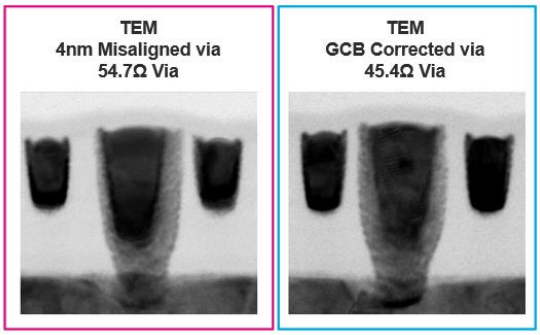


Fig. 7. Left - TEM of an intentionally misaligned via with Kelvin via resistance of 54.7Ω. Right -TEM of misaligned via with GCB correction and via resistance of 45.4Ω. The via is now well centered in the line.