Landing-Pad Geometry Engineering for Contact-Access Margin

AVS72 Supplemental Figure - Manufacturing Science & Technology Poster Session - public patent figures, qualitative FMEA, validation roadmap

No unpublished recipe | no node-specific dimensions | no product/yield claim

A. Public patent figures used as the structural basis

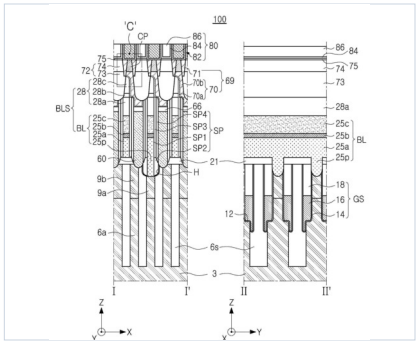

Fig. 3a - cell stack context: BL, contact plug, LP structure, capacitor connection, cell-gate stack.

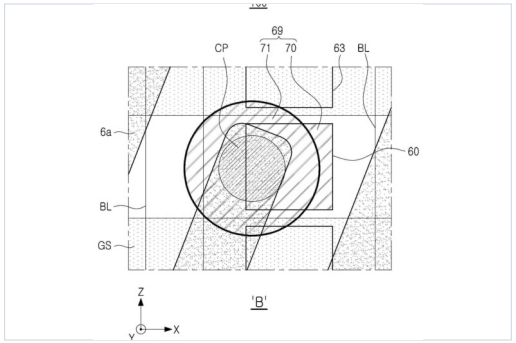

Fig. 4a - plan-view LP/CP/BL/GS layout; highlights lateral access/overlap design space.

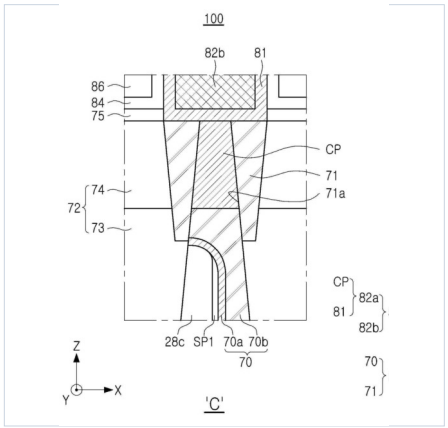

Fig. 4b - enlarged LP cavity and conductive-pattern region; CP is inside upper-LP cavity and connects to lower-electrode/barrier region.

Technical abstraction

Patent-visible geometry is converted into a **manufacturing variable**:
- upper LP cavity + conductive pattern (CP)
- LP / lower-electrode contact-access path
- side + top interface contribution
- tolerance to local overlay/profile variation

Output of the supplemental figure: define what should be measured, not claim measured improvement.

Source: cropped public KR patent publication 10-2024-0135997, Figs. 3a/4a/4b. Patent labels retained. No process recipe, CD, thickness, or node is added.

B. Premise and mechanism chain

Problem: scaled cell-array contact stacks become sensitive to capacitor-electrode shift, landing-area loss, local CMP/topography variation, and contact-interface geometry.
Mechanism: LP cavity / CP placement -> additional contact-access geometry -> less sensitivity to local placement/profile variation -> narrower Rc/leakage/C distribution tails.
Positioning: this is a public-disclosure-based manufacturing framework, not a product implementation or yield claim.

C. Detailed qualitative FMEA and validation map

Failure mode	Root cause / sensitivity	Observable signature	Validation use
Electrode-to-LP shift	Overlay error; local LP/cavity profile variation	Reduced landing overlap; Rc tail; contact fail	Overlay map + cross-section SEM/TEM -> landing-window budget
Effective contact-area loss	CP/upper-LP geometry not fully captured by lower electrode	Contact resistance broadening; Kelvin-chain tail	Contact-area extraction; CP/LP profile split
CMP/topography nonuniformity	LP height spread, dishing/erosion, local step variation	Upper-LP/cavity height distribution; profile asymmetry	Height/CD metrology + CMP/process split
Interface/liner discontinuity	Barrier/liner continuity at top/side interface	Rc spread, leakage tail, capacitance distribution spread	Electrical monitor split; leakage/C statistics
Parasitic/array-tail risk	Geometry-dependent local C/R coupling and pattern variability	RC model spread; array-tail sensitivity	Parasitic extraction + process/device sensitivity model

D. Validation roadmap - how the concept becomes measurable without confidential data

1. Structure
SEM/TEM; LP/cavity/CP profile; lower-electrode contact geometry

>

2. Metrology
CD/overlay; local height; landing/contact-area extraction; cavity taper

>

3. Electrical
Rc monitor; Kelvin/contact chain; leakage/C distribution; tail analysis

>

4. Sensitivity
overlay split; CMP/topography split; etch/profile split; process window

>

5. Modeling
geometry-to-area model; RC extraction; failure-mode sensitivity map

Boundary: public patent figures and public-disclosure language only. No unpublished process recipe, Samsung affiliation/product implementation, node-specific dimension, CD/thickness/etch/CMP condition, measured yield improvement, step-count claim, or internal roadmap. All FMEA entries are qualitative and used to define validation needs.

Upload as supplemental 1-page PDF with AVS72 abstract; keep title/abstract unchanged unless final IP/legal review requests edits.