Advanced Microelectronic Materials and Devices Mini-Symposium
Room 318 - Session AM+EM+TF-ThA
ALD Fundamentals to Devices

Moderators: Himanandhan Reddy Kottur, University of Florida, **Andrew Meng**, University of Missouri

2:15pm **AM+EM+TF-ThA-1 When Growth Has Not Yet Begun: Nucleation and Interface Control in Atomic Layer Deposition***, **Zsófia Baji,*** Centre for Energy Research, Hungary*; Zsófia Bérces,* Centre for energy research, Hungary*; Zoltán Szabó,* Centre for Energy Research, Hungary **INVITED**

Atomic layer deposition (ALD) is generally described as a self-limiting thin-film growth technique producing conformal and compositionally controlled layers with atomic-scale precision. However, in the earliest stages of growth, precursor adsorption, surface chemistry, and substrate-dependent reaction pathways limit growth. These phenomena become increasingly important in the deposition of ultrathin functional films for emerging electronic technologies, where the target thickness often lies entirely within the nucleation regime. Understanding the atomistic and chemical mechanisms governing the transition from isolated nuclei to continuous films is therefore essential for the development of next-generation memory, logic, and two-dimensional device architectures.

The classical nucleation behaviour of oxide ALD systems is largely influenced by the chemistry and crystallinity of the substrates: the initial ALD cycles are controlled not only by precursor saturation but also by the density and distribution of chemically active surface sites and lattice matching. The role of precursor size, ligand configuration, and available hydroxyl density in determining growth-per-cycle behaviour and nucleation efficiency can be examined using phenomenological nucleation models. The comparison between experimental film morphologies and theoretical growth descriptions give insight to the initial stages of film growth. Mathematical nucleation modelling used to analyse the transient growth behaviour can be used to derive the unknown boundary conditions governing the initial deposition stages.

The difference between precursor chemistries can be demonstrated by oxide and sulfide nucleation pathways. Sulfide growth is fundamentally hindered by the mismatch between conventional hydroxyl-terminated oxide substrates and sulfur-based film chemistry, therefore sulfide ALD repeatedly re-enters a renucleation regime during the early cycles, resulting in delayed film closure and poor ultrathin continuity.

To overcome these limitations, different nucleation-enhancement treatments can be employed to increase the density of reactive surface sites and enhance nucleation. The hydroxylation of the surface enhances the nucleation of oxide films, while controlling other growth chemistries requires a chemically engineered approach for the targeted functionalisation surfaces. Thus, nucleation must be considered as an interface-controlled process governed by the compatibility between precursor chemistry and surface termination.

2:45pm **AM+EM+TF-ThA-3 MoO_2Cl_2 as an alternative Mo ALD Precursor for MoS_2 with Improved Thin Film Properties***, **Nihal Khatiwoda,*** University of Michigan*; Ian Campbell,* IMEC USA*; Pierre Morin,* IMEC Belgium*; Benjamin Groven,* IMEC, Belgium*; Ageeth Bol,* University of Michigan

ALD of MoS_2 is a promising route for scalable and conformal synthesis of 2D semiconductors for nanoelectronics applications. However, it is often limited by small grain sizes and out-of-plane features, which degrade device electrical properties. In this work, we investigate MoO_2Cl_2 as a novel molybdenum precursor for ALD of MoS_2. Compared to conventional Mo precursors, MoO_2Cl_2 exhibits enhanced vapor pressure, leading to more efficient precursor delivery. Additionally, its chlorine-based chemistry introduces the possibility of in-situ etching which can help suppress undesirable nucleation, out of plane growth, and thus facilitate lateral expansion of domain features.

Both thermal and plasma-enhanced ALD processes were developed using MoO_2Cl_2 and H_2S as co-reactant. For the thermal process, a stop-flow approach was implemented to increase co-reactant residence time and enhance the reaction kinetics.

In-situ spectroscopic ellipsometry reveals that MoO_2Cl_2 exhibits a substrate enhanced transient growth regime during the initial ALD cycles, characterized by rapid nucleation. This is followed by a slower homo-deposition growth where the system enters a steady state growth regime. This behavior suggests the possibility of tailoring the precursor-substrate chemistry to reduce nucleation density and enhance lateral growth.

Ex-situ characterizations further support the effectiveness of this precursor system. XPS confirms the absence of chlorine incorporation in the resulting films, indicating clean ligand removal and absence of unwanted chlorine doping into the films. AFM reveals improved surface morphology with increased grain size and, notably, absence of out-of-plane features.

Overall, this study demonstrates that MoO_2Cl_2 is a promising precursor for ALD of high-quality MoS_2. Its favorable volatility, combined with chlorine-mediated surface chemistry, enables improved control over film morphology and crystallinity. These findings highlight a viable pathway toward overcoming longstanding challenges in ALD MoS_2 growth, advancing its potential for integration into next generation nano-electronic devices.

3:00pm **AM+EM+TF-ThA-4 Impact of Ti Adhesion Layer and ALD Al_2O_3 Thickness on Interfacial Energy Barriers in metal/insulator/metal (MIM) Devices***, Jessica Haglund, **John Conley,*** Oregon State University

Control and understanding of interfacial energy barriers at metal insulator contacts is essential for designing MOS and MIM based devices. These barriers depend not only on the details of the metals and dielectrics used, but also on processing conditions, deposition order, and structure of the interface. To use noble metal electrodes, a thin interfacial metal is essential for good adhesion. Thin interfacial metals have also been investigated as a way to tailor barrier heights. Ultrathin dielectrics are needed for MOS gates and high capacitance MIM capacitors. However, the dielectric constant, density, and optical refractive index of ALD Al_2O_3 have all been reported to be a function of film thickness. In this work, we investigate the impact of Ti adhesion layer and ALD Al_2O_3 film thickness on interfacial electron energy barriers in Pt/Ti/Al_2O_3/TiN MIM devices.

100 nm TiN bottom electrodes were reactive ion sputtered. ALD with TMA and H_2O was used to deposit Al_2O_3 using 50, 75, 100, 125, 150, 175, and 200 ALD cycles in a Picosun R150 and 100 and 200 cycles in a Picosun R200. Following ALD a thin Ti IL (0.5, 1, 2, 5, 10 nm) and a 10 nm Pt top electrode were deposited via electron beam evaporation using a shadow mask. CV and IV measurements were taken on the completed MIM structures. Energy barriers were measured suing internal photoemission (IPE) spectroscopy using a house-built system.[1] Top gate voltage was swept from 0 to 2 V and 0 to -2 V using 0.1 V steps. At each bias, incident photon energy was swept from 1.7 to 5.5 eV. IPE thresholds were determined at each voltage using yield plots and zero field barriers were determined using Schottky plots.

Both the top Pt/Al_2O_3 and bottom TiN/Al_2O_3 electron barriers were a function of Al_2O_3 thickness. While both electron barriers were roughly constant at ~3.6 eV for Al_2O_3 films ≥ 12 nm thick, both decreased by roughly 0.5 eV as Al_2O_3 thickness decreased down to 5 nm. For Ti, a 0.5 to 1.0 nm thick interfacial layer was sufficient to completely dominate the electron energy barrier of the Pt/Ti stack. Insertion of a Ti layer also resulted in band tailing, likely due to oxygen scavenging, but had no impact on the bottom Al_2O_3/TiN electrode barrier. The degradation of electron barriers with insulator thickness and dominance by a very thin layer of metal at the interface are important considerations for the prediction and optimization of leakage currents and performance in these devices. Additional measurements on Ga_2O_3 will be discussed.

[1] J. Haglund, T. Mimura, J.F. Ihlefeld, and J.F. Conley, Jr., ACS Appl. Electron. Mater. **6**(5), 3249–3256 (2024)

3:15pm **AM+EM+TF-ThA-5 Evaluation of Barium-Based Precursors for Atomic Layer Deposition of Barium Titanate Thin Films***, **Aenakshi Sircar,*** Boise State University*; Peter Micah,* boise State University*; Steven Hues, Elton Graugnard,* Boise State University

Atomic Layer Deposition of Barium titanate (BTO) has been a topic of interest for its potential application in high-k dielectric and ferroelectric material for energy-efficient logic and low-voltage memory devices. It is a perovskite ferroelectric with a low coercive field and switchable polarization at room temperature. Several deposition methods have been explored for integrating conformal BTO thin films into high-aspect-ratio structures for advanced memory applications. Among these, atomic layer deposition (ALD) stands out due to its ability to achieve highly conformal low-temperature growth through self-limiting surface reactions using reactive precursors. Despite these advantages, the development of a comprehensive ALD process for barium titanate remains challenging, particularly due to the limitations associated with barium precursor chemistry. The low volatility and poor thermal transport of many barium-based precursors limit the ALD process window. Additionally, most barium-

based precursors are extremely hygroscopic in nature and often form $Ba(OH)_2$, which can readily react with carbon-containing compounds to form $BaCO_3$. This introduces unfavorable conditions for the formation of BTO, since $BaCO_3$ and TiO_2 require higher energy to form BTO compared to $Ba(OH)_2$ and TiO_2. This behavior further complicates film characterization and can also negatively impact the electrical properties of the films.

Here, we report progress toward precursor selection for carbon-free barium titanate deposition. We investigate three different barium-based precursors: isopropyl [$Ba(iPr_3Cp)_2$], tertbutyl [$Ba(tBu_3Cp)_2$], and a novel imidazolate-based precursor, [Ba-Zttt]. The deposition cycles are optimized over several parameters, including the ALD temperature window (250–350 °C), growth per cycle, and film structure. The films are further characterized for thickness, density, roughness, phase composition, and dielectric properties to assess the feasibility of the different precursors for ALD of BTO and their potential contribution toward quaternary barium-based oxides.

3:30pm **AM+EM+TF-ThA-6 Deposition of Metastable ZrO_2 Crystalline Films at Low Temperatures by Electron-Enhanced Atomic Layer Deposition (EE-ALD)***, Zachary Sobell,* ***Steven George***[1]*,* University of Colorado at Boulder

The metastable cubic and tetragonal ZrO_2 crystalline phases are important as high-k dielectric materials.Electron-enhanced atomic layer deposition (EE-ALD) was used to grow metastable ZrO_2 crystalline films with thicknesses of ~30 nm at low temperatures < 100 °C.This EE-ALD process employed alternating exposures of tetrakis(ethylmethylamido)zirconium (TEMAZr) and low energy (~70-100 eV) electrons concurrent with an oxygen (O_2) reactive background gas (RBG).ZrO_2 EE-ALD displayed rapid nucleation on silicon native oxide and linear growth in the steady state region.

The ZrO_2 EE-ALD was performed using an electron beam from a hollow cathode plasma electron source (HC-PES) with sample currents of ~30 mA over 10 cm^2.The electron beam can desorb surface species by electron stimulated desorption.The electron beam also travels through the O_2 RBG in the reactor at pressures of ~1-3 mTorr.Electron induced dissociation can form ions and radicals that facilitate the growth and oxidation of the ZrO_2 film.In addition, a negative bias voltage (-30 V) can be applied to the sample.This negative bias is believed to pull positive ions to the surface to enhance the film crystallinity and refractive index (RI).

With no applied sample bias and 5 s electron exposures, ZrO_2 EE-ALD proceeded at 1.2 Å/cycle and displayed an RI of 1.63 at 589 nm. Moderate crystallinity was observed by grazing incidence X-ray diffraction (GI-XRD) as shown in **Figure 1**. Increasing the electron exposure time increased the crystallinity and RI. A 10 s electron exposure increased the RI to 1.75. The crystallinity also increased significantly as displayed in **Figure 2**.The ZrO_2 EE-ALD growth rate was measured at 0.8 Å/cycle.

For the shorter electron exposure of 5 s, the application of a -30 V sample bias also increased the RI and crystallinity slightly versus no bias.The RI was measured at 1.70 and the EE-ALD growth rate was 0.8 Å/cycle. Increasing the electron exposure to 15 s with the simultaneous application of a -30 V bias increased the RI further and produced the most pronounced crystallinity as shown in **Figure 3**.A growth rate of 0.9 Å/cycle was measured along with an RI of 1.9.

The crystallinity and RI of the metastable ZrO_2 crystalline films with thicknesses of ~30 nm grown by EE-ALD depends on electron beam exposure time and negative sample bias voltage.The primary incident electrons may increase film crystallinity and RI by enhancing surface atomic mobility.The negative sample bias voltage may increase crystallinity and RI by facilitating oxidation by attracting O_2^+ positive ions to the sample.

3:45pm **AM+EM+TF-ThA-7 Zirconium Phosphate ALD Electrolyte for TiO2-Channeled H+ ECRAM***, John Hoerauf, David Stewart,* University of Maryland, College Park*; A. Alec Talin,* Sandia National Laboratories, USA*; Gary Rubloff,* University of Maryland, College Park

Artificial Intelligence (AI) computing energy demands are on pace to surpass global energy production. Analog in-memory computing (IMC) hardware development represents a paradigm shift to reduce the energy required for these calculations by up to six orders of magnitude. Electrochemical RAM (ECRAM) is a promising non-volatile three-terminal transistor technology to realize physical neuromorphic IMC circuits. To program information, ECRAM utilizes reversible electrochemical reactions between the gate and drain terminals to change the conductance of the channel material between the source and drain terminals, representing the state of information during read-out. ECRAM transistors that utilize H^+ as the electrochemically active species are compatible with CMOS devices, offer faster programming speed, and have increased cycle durability compared to Li^+ ECRAM. Due to the mobility of protons, H^+ ECRAM also provides an excellent platform for studying the underlying phenomena that govern informational state retention across all ECRAM chemistries, but further studies require a solid-state electrolyte with properties not yet reported in thin-film electrochemistry.

Zirconium Phosphate (ZrP_xO_y) is a promising electrolyte with the requisite properties, including a composition-dependent H^+ conductivity. This presentation discusses a novel atomic layer deposition (ALD) development for ZrP_xO_y and the successful application of this thin-film electrolyte in H^+ ECRAM. ALD ZrP_xO_y was deposited using both super-cycling and phosphate plasma polymerization to alter the phosphorous to zirconium ratio between 1.5:1 and 4.2:1. This change in composition resulted in a one decade change in proton conductivity (3e-10 to 4e-9 S/cm) while exhibiting electronic conductivities below the measurement resolution limit (<1e-11 S/cm), ideal for studying state retention in ECRAM. The higher conductivity $ZrP_{2.6}O_{6.6}$ electrolyte was applied to an ECRAM singe-transistor platform that utilizes TiO_2 between the source and drain for readout. Two decades of programming range were demonstrated with a projected 4-hour state retention time. This represents the first successful demonstration of a full solid-state H^+ ECRAM transistor with an anhydrous ALD electrolyte. Additionally, a novel electrochemically-induced phase transition at the composition $H_{0.01}TiO_2$ was observed in Titania, as confirmed both through cyclic voltammetry and a metal-to-insulator behavior between the source and drain terminals. This phase transition is similar to that observed in the Li-TiO_2 system and is the key to understanding how H^+ conductivity in the electrolyte affects informational state retention in future studies.

4:00pm **AM+EM+TF-ThA-8 Work-Function Metal Engineering for Gate-All-Around Logic Devices: Materials, Integration Challenges, and Pathways for Future Technology Nodes***, Ganesh Dindukurthi,* ASM America

Gate-all-around (GAA) nanosheet transistors offer the electrostatic control needed to extend logic scaling beyond FinFETs. However, their three-dimensional geometry leaves little space for the replacement metal gate stack. Future devices must also support several threshold-voltage options to balance speed, power, and leakage. These demands make work-function-metal (WFM) engineering an important challenge for upcoming technology nodes.

In a GAA transistor, threshold voltage is not determined by the metal alone. It also depends on interactions with the high-k dielectric, interfacial layer, and barrier materials. Oxygen vacancies, interface dipoles, elemental diffusion, and thermal processing can shift the effective work function. This explains why results from blanket films or capacitor structures may not carry over directly to nanosheet devices. A suitable WFM must provide the required work function while maintaining low resistance, low leakage, minimal electrical-thickness penalty, thermal stability, and uniform nanosheet coverage.

One direction for future nodes is to simplify the gate stack. Separate n-type and p-type metals are currently combined with dielectric dipoles to create multiple threshold voltages. As dimensions shrink, a weak-n or midgap metal could serve as a common starting point, while controlled dipoles shift the work function toward the required NMOS or PMOS values. This may reduce the number of patterned metal layers, but it requires tighter control of dipole strength, interface quality, and device variation. Another option is to pair a strong p-type metal with n-type dipole tuning, particularly if p-type dipoles continue to affect electrical thickness or mobility.

How these materials are placed is just as important as the materials themselves. Repeated metal and dipole patterning consumes gate space and can introduce etch damage, unwanted dipoles, and threshold-voltage variation. Additive patterning and area-selective deposition may help by placing tuning materials only where needed. Their success will depend on maintaining selectivity and clean interfaces through cleaning, annealing, and material removal.For 1.4 nm, 1.0 nm, and later nodes, work-function engineering should be viewed as a gate-stack integration problem rather than a search for a single new metal. Progress will depend on combining a stable, low-resistance WFM with controlled dielectric interfaces, diffusion barriers, and dipole layers. Improvements seen during material screening must translate into consistent threshold voltage, mobility, reliability, and gate resistance in the final device.

[1] **JVST Highlighted Talk**

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