Supporting figures.

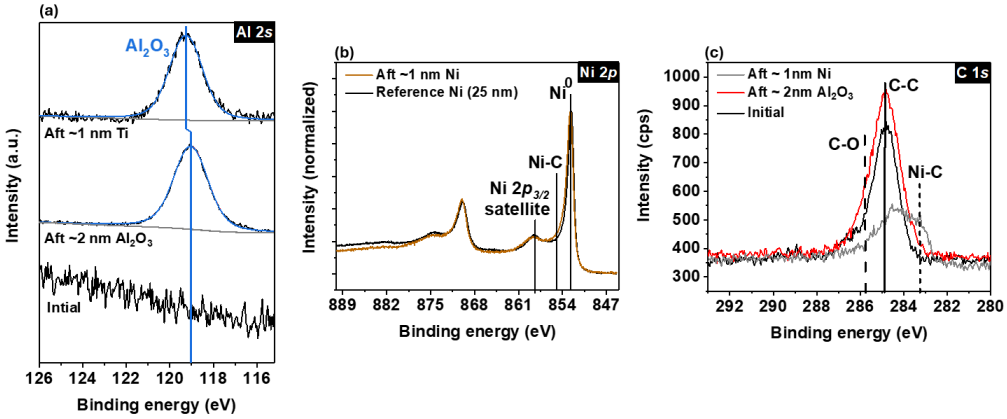

FIG 1. *In situ* XPS of Ni/ Al_2O_3/ β-Ga_2O_3 stack. (a) Al 2*s* and (b) Ni 2*p* and (c) C 1*s* core level, of initial (as-loaded), after ~ 2nm Al_2O_3 deposition and after ~ 1nm Ni deposition, showing interface reactions caused by Ni gate. (Al 2*s* is used for fitting due to an overlap between Ni 3*p* and Al 2*p* regions.)

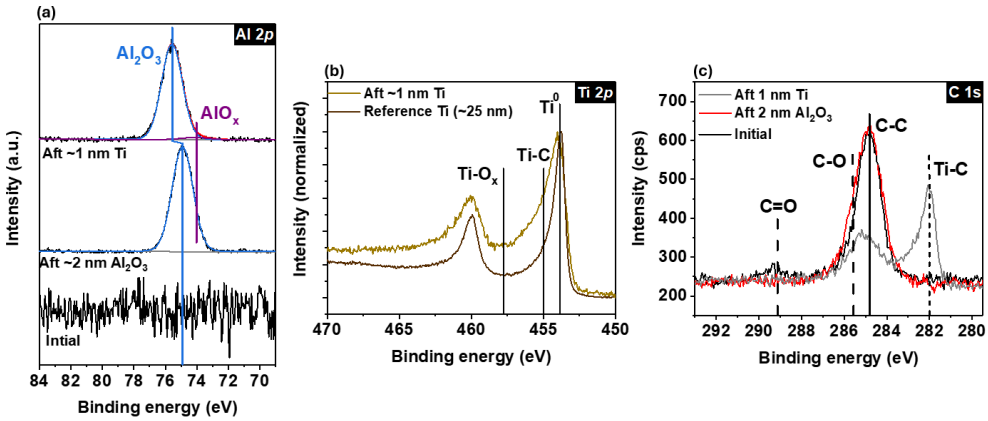

FIG 2. *In situ* XPS of Ti/ Al_2O_3/ β-Ga_2O_3 stack. (a) Al 2*p* and (b) Ti 2*p* and (c) C 1*s* core level spectra, of initial, after ~ 2nm Al_2O_3 deposition and after ~ 1nm Ti deposition, showing interface reactions caused by Ti gate.

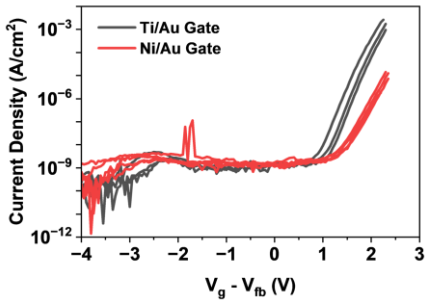

FIG 3. Normalized gate leakage for β-Ga_2O_3-based MOSCAPs with ~12 nm of Al_2O_3 and Ti/Au or Ni/Au gate, where a lower leakage in the accumulation region of Ni gate devices is compatible with a more robust dielectric layer.