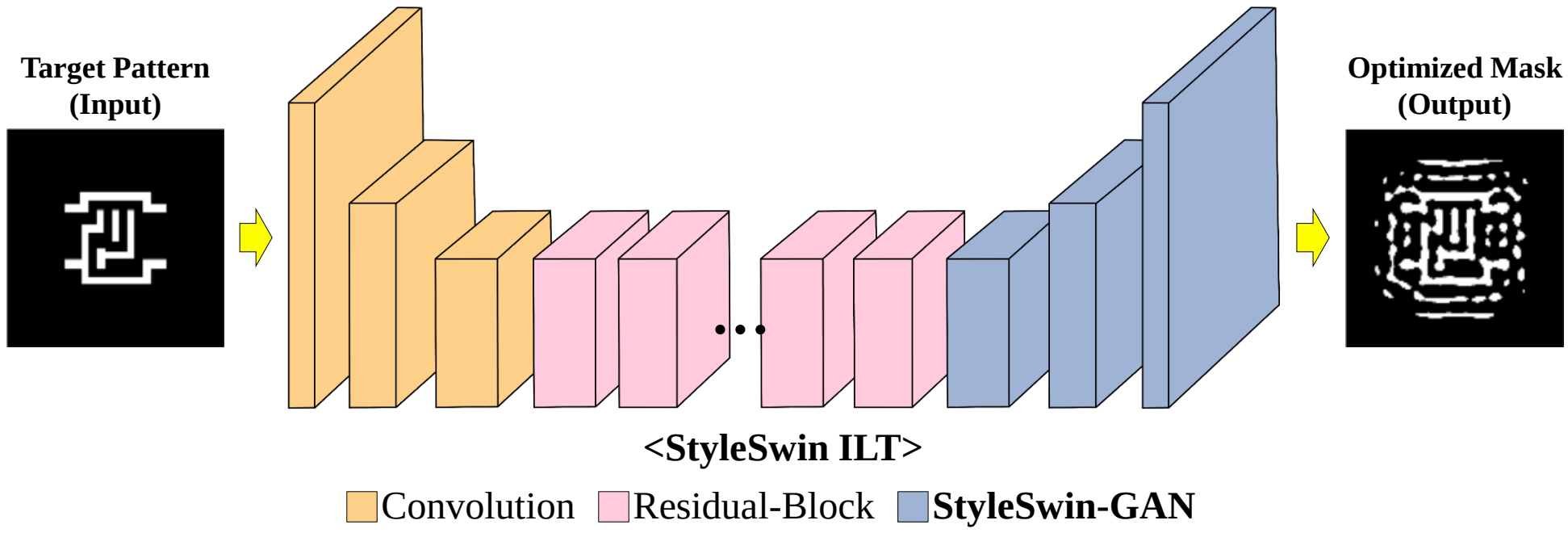

Figure.1 Overall architecture of the proposed StyleSwin[1]-based ILT model, built upon DAMO ILT[2]. The target pattern (input) is processed via convolution and residual blocks, then passed to the StyleSwin-GAN stage to produce the optimized mask.

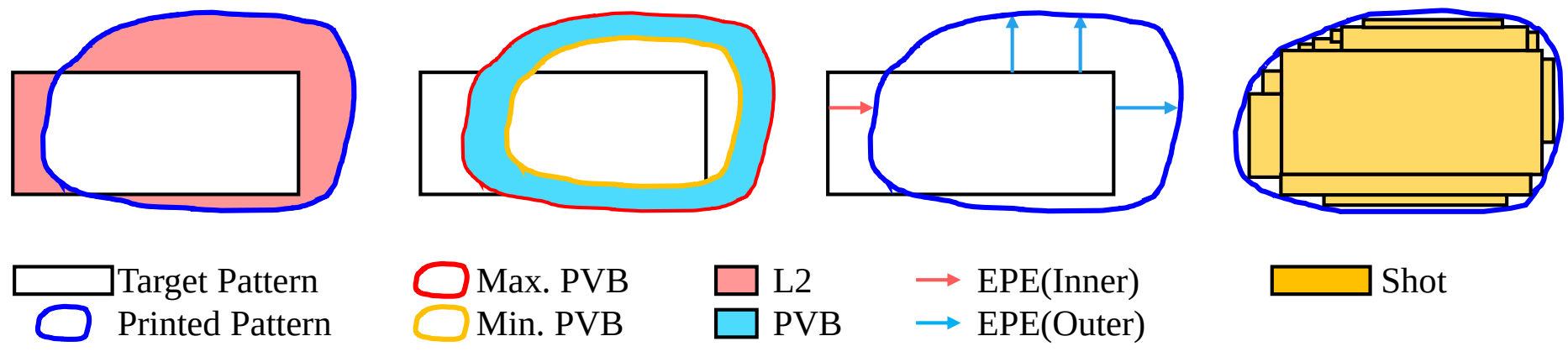

Figure.2 Visualization of the evaluation metrics. (a) **L2 error** captures the pixel-level discrepancy between the nominal print and the intended design. (b) **PVB** represents the maximum pattern variation across different process conditions. (c) **EPE** measures how far the actual edges deviate from the target edges. (d) **#Shots** counts the rectangular exposures needed to form the mask.

Table.1 Comparison of mask optimization results on the LithoBench[3] MetalSet dataset.

Metrics	GAN-OPC[4]	CFNO[5]	Neural-ILT[6]	DAMO[2]	StyleSwin(ours)
L2↓	43414	47814	36670	**32579**	33754
PVB↓	41290	46131	42666	**41173**	42373
EPE↓	8.7	12.5	7.3	**5.4**	**5.4**
Shots↓	574	**302**	476	523	500

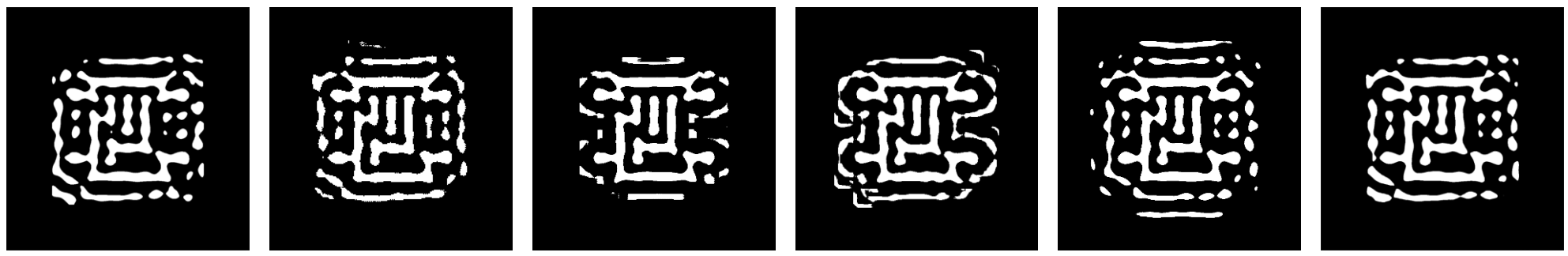

Figure.3 Mask Optimization for MetalSet Patterns of LithoBench (a)Ground Truth, (b)GAN-OPC, (c)CFNO, (d)Neural-ILT, (e)DAMO, (f)StyleSwin(ours)

References

[1] Zhang, Bowen, et al. "Styleswin: Transformer-based gan for high-resolution image generation." *Proceedings of the IEEE/CVF conference on computer vision and pattern recognition*. 2022.

[2] Chen, Guojin, et al. "DAMO: Deep agile mask optimization for full chip scale." *Proceedings of the 39th International Conference on Computer-Aided Design*. 2020.

[3] Zheng, Su, et al. "Lithobench: Benchmarking ai computational lithography for semiconductor manufacturing." *Advances in Neural Information Processing Systems* 36 (2023): 30243-30254.

[4] Yang, Haoyu, et al. "GAN-OPC: Mask optimization with lithography-guided generative adversarial nets." *Proceedings of the 55th Annual Design Automation Conference*. 2018.

[5] Yang, Haoyu, and Haoxing Ren. "Enabling scalable AI computational lithography with physics-inspired models." *Proceedings of the 28th Asia and South Pacific Design Automation Conference*. 2023.

[6] Jiang, Bentian, et al. "Neural-ILT: Migrating ILT to neural networks for mask printability and complexity co-optimization." *Proceedings of the 39th International Conference on Computer-Aided Design*. 2020.

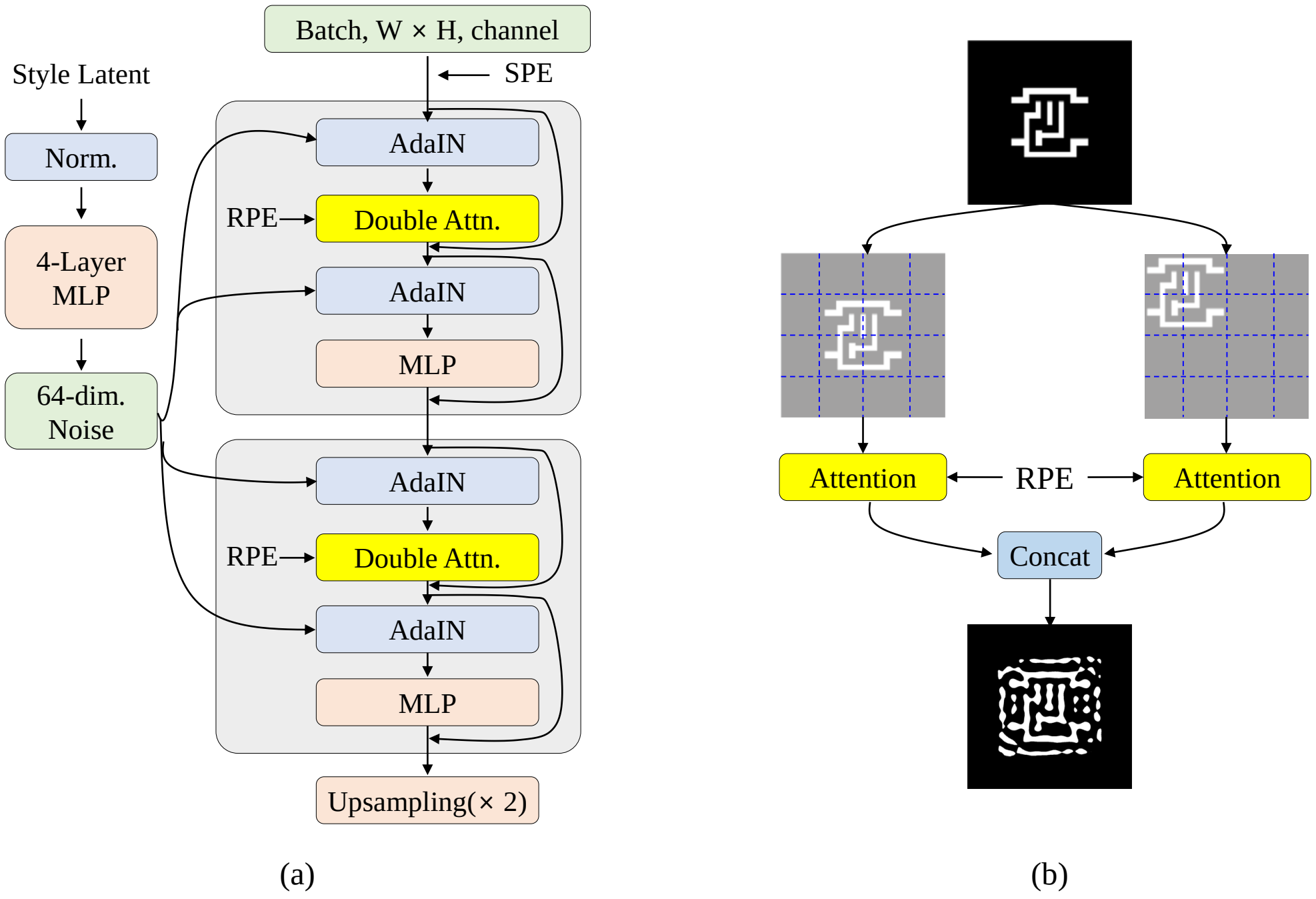

Figure.4 Overview of the StyleSwin[1] architecture for ILT. (a) Schematic of the StyleSwin block borrowed in this work. It combines SPE (Sine Positional Encoding) and RPE (Relative Positional Encoding) to capture positional information, while AdaIN (Adaptive Instance Normalization) incorporates the 64-dimensional noise derived from a style latent. (b) Example illustration of the block's double attention (regular + shifted). Two window-based attentions run in parallel and their outputs are concatenated to form the final feature map.

References

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[2] Chen, Guojin, et al. "DAMO: Deep agile mask optimization for full chip scale." *Proceedings of the 39th International Conference on Computer-Aided Design*. 2020.
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