Thin Films
Room 206 B W - Session TF+CPS+MS+EM-ThA

Thin Films for Microelectronics II

Moderators: Lauren Garten, Georgia Institute of Technology, **Christophe Vallee**, University at Albany

2:15pm **TF+CPS+MS+EM-ThA-1 Area Selective Deposition Processing in the Memory Industry: How to Take Advantage of the High-Volume Manufacturing Environment***, **Francois Fabreguette**, Jeff Hull, Huicheng Chang, Erik Byers, Gurtej Sandhu,* Micron Technology **INVITED**

Aggressive scaling from node to node in the memory industry has led to a paradigm shift towards Area Selective Deposition (ASD) technique to overcome traditional processing challenges. For example, punches or etches not being capable anymore in High Aspect Ratio structures >100:1 can be replaced by selective deposition processes on the sidewall only, eliminating the need to clear a bottom contact. Likewise, ASD can be used to heal a contact seam that can easily form when the deposited metal pinches off at the top of a High-Aspect ratio structure, leavinga void in the middle of the filled contact. Finally, in tiered structures used for 3D memory scaling, ASD allows for dielectric re-deposition on one tier type selective to the other tier type for cell sculpting without any critical dimension penalty.The present abstract covers a few examples of ASD processes developed in Micron High Volume Manufacturing environment:The state-of-the-art 300mm wafer tooling capability as well as multiple full-wafer inline metrology techniques (such as X-Ray fluorescence, X-ray Photoelectron Spectroscopy, X-Ray Reflectivity, Ellipsometry, Atomic Force Microscopy) allows to characterize the loss of selectivity on the non-growth surfaces on wafer-level. This provides across-wafer inhibition efficiency, which is criticalfor Area Selective Deposition future adoption in large scale production. The case study of ASD TiN using new high-temperature oxide inhibitors is presented. The systematic inline metrology characterization of the inhibited blanket oxide surfaces after TiN deposition at various temperatures is used to determine the best selectivity conditions as well as individual inhibitor performance benchmarked to the best-known oxide inhibitor typically used in the ASD community. Besides, Fourier Transform Infrared (FTIR) spectroscopy, Water Contact Angle measurements (WCA) and carbon content from XPS measurements were performed immediately after inhibition. Theyprovided the surface signature of each inhibitor and were correlated to their overall inhibition efficiency.

2:45pm **TF+CPS+MS+EM-ThA-3 High-Throughput MLD Screening of Photoresists for EUV Lithography via UV and E-Beam Exposure***, **Duncan Reece**, David Bergsman,* University of Washington

As semiconductor patterning pushes toward sub-5 nm features, next-generation photoresists must deliver high resolution, environmental and chemical stability, and compatibility with extreme ultraviolet (EUV) lithography processes. However, EUV photoresist materials explored to date still face challenges such as ease of deposition and achieving sub-nanometer chemical uniformity. Molecular layer deposition (MLD) offers precise control over thin-film structure and composition, enabling the design of hybrid materials tailored to meet these challenges. Previous work has demonstrated MLD-based EUV photoresists incorporating aluminum (Al) and tin (Sn); however, the influence of the organic reactant on the final photoresist properties remains largely underexplored. Using our custom high-throughput multi-chamber MLD system, we synthesized 18 organic–inorganic hybrid films from two organometallic precursors—trimethylaluminum diethylzinc, and tetrakis(dimethylamino)tin(IV)—paired with six organic linkers: hydroquinone bis(2-hydroxyethyl) ether, 1,2,4-trihydroxybenzene, 1,5-hexadiene-3,4-diol, 2-butyne-1,4-diol, cis-2-butene-1,4-diol, and 3,4-dihydroxy-1-butene. Film candidates were screened for growth rate, ease of deposition, uniformity, and ambient stability. To assess potential photochemical reactivity, UV-induced crosslinking, or structural rearrangement, we measured thickness changes before and after solvent exposure, both with and without deep UV treatment.Selected high-performing films were subjected to electron beam lithography as a stand-in for EUV testing, followed by development to evaluate feature resolution and pattern fidelity using scanning electron microscopy and profilometry. Mechanical durability was assessed via nanoindentation, while chemical transformations were characterized with Fourier Transform Infrared Spectroscopy (FTIR) and X-ray Photoelectron Spectroscopy (XPS).Our results identify material systems that combine robust environmental and chemical resistance with promising lithographic performance and photo-reactive behavior. While EUV lithography remains the ultimate target application, e-beam serves as a high-resolution surrogate to guide photoresist development. This integrated approach demonstrates the power of high-throughput MLD and multi-parameter screening for accelerating the discovery of advanced materials for next-generation lithographic technologies.

3:00pm **TF+CPS+MS+EM-ThA-4 Physical Modeling of Side Wall Deposition by Inclined Electron Beam Evaporation***, **Yujia Liu**, Ina Ostermay, Andreas Thies, Olaf Krüger,* Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany

Three-dimensional nanostructures like bars, fins and holes are essential design features in modern semiconductor processing to overcome traditional design limits and achieve More-than-Moore device density. Inclined electron beam evaporation is commonly applied for material deposition on these nanostructures to reach conformal step coverage on side walls. These thin films could serve as seed layers for electroplating, applied for p-contacts of GaAs diode bars[1], air bridges for source pads or through substrate VIA contacts in GaN transistors[2,3]. Depending on the exact nanostructure forms, shadowing can be a challenge for decent step coverage. Both experimental and modeling results show an improvement in conformality by optimizing inclination angles[4–6].

In this study, a physical model is developed to predict the step coverage on the side walls of different structures by inclined evaporation. We will present our model based on several general conditions: a. the evaporation is under high vacuum (below 10^{-5} mbar); b. evaporation beam is perpendicular to the wafer by 0° inclination (fig. 1): c. wafers are rotated during evaporation; d. the film density is independent of inclination – in reality, the film could become porous when inclined[7]. Within the model, evaporation on bar structures is firstly simulated, revealing no shadowing (fig. 2a). The conformality over the inclination and the taper angles are calculated and plotted in fig. 2b. Calculated data are in good agreement with experimental results. The demonstrative cross-section of the inclined evaporation on a bar structure with 90° side wall is shown in fig. 2c. Next, the model is developed for the shadow effects within circular or square holes (fig. 2d,g). For circular holes, the dependence of evaporation shadowing on the inclination angle as well as an exemplary distribution of deposition rate at 30° inclined evaporation over the rotation angles are illustrated in fig. 2e. The conformalities over the depths for different inclination angles are plotted in fig. 2f. For a square hole, the computed conformality distribution on one side wall is illustrated in fig. 2h for 60° inclined evaporation. The experimental result of the inclined evaporation (fig. 2i) shows the same triangle pattern as the modeling result.

Our model allows prediction of the step coverage on the side wall during inclined electron beam evaporation in order to select the inclination for the evaporation on three-dimensional nanostructures. With the help of this model, we can also forecast the layer conformality for various nanostructures of different sizes evaporated at the same time and, hence to create a design manual.

3:15pm **TF+CPS+MS+EM-ThA-5 Highly Ordered NiO (111) Films on Sapphire Substrates via Low-Temperature Hollow Cathode Plasma-ALD and Their Post-Deposition Annealing Characteristics***, Fatih Bayansal, Steven Allaby, Habeeb Mousa, Helena Silva, **Necmi Biyikli**,* University of Connecticut

Nickel oxide (NiO) is a promising p-type wide band gap semiconductor material for next generation optoelectronic and energy devices. In this study, the growth process and thermal annealing behavior of NiO thin films grown on c-plane sapphire substrates by hollow-cathode plasma-assisted atomic layer deposition (HCP-ALD) method were investigated. $NiCp_2$ was used as the nickel precursor heated at 100°C, and O_2 plasma was preferred as the oxidizing agent under 100W rf-power and 20 sccm flow rate. The films were grown within a substrate temperature range of 100 – 250°C.

The obtained film samples showed high transmittance in the visible spectrum and exhibited strong absorption in the UV spectrum. Optical band gap values determined by Tauc analysis were found between 3.54 and 3.59eV. The refractive indices increased with the growth temperature and reached 2.38, while the extinction coefficient and film porosity decreased for higher temperature films. X-ray diffraction (XRD) analyses revealed that the films exhibit a highly textured structure with exclusive (111) orientation. No peaks belonging to any other phase or crystal plane were observed. Moreover, grazing incidence XRD (GIXRD) measurements showed no detectable peaks, confirming the monocrystalline film character, and suggesting a surface-parallel alignment and potentially dense and thin film morphology. In addition, shifts in the diffraction peaks were observed depending on the growth temperature.

In order to evaluate the thermal stability and performance of the films, the samples grown at 250°C were annealed at 300, 350 and 400°C. Ongoing studies include characterization of electrical properties (Hall effect) such as carrier density, mobility and conduction type as well as crystal structure (XRD, TEM) and chemical composition (XPS). This holistic approach will contribute to understanding the impact of post-deposition annealing on the crystal quality and charge transport properties of NiO films.

This work contributes to the development of optimized p-type oxide semiconductors for transparent electronics and heterojunction-based devices through controlled low-temperature ALD process and post-deposition thermal engineering.

3:30pm **TF+CPS+MS+EM-ThA-6 Textured Growth and Electrical Characterization of Zinc Sulfide on Back-End-of-the-Line (BEOL) Compatible Substrates**, ***Claire Wu***, *Mythili Surendran, Anika Priyoti, Gokul Anilkumar,* University of Southern California*; Chun-Chen Wang,* Taiwan semiconductor Manufacturing Company, Taiwan*; Cheng-Chen Kuo, Cheng-Hsien Wu,* Taiwan Semiconductor Manufacturing Company, Taiwan*; Rehan Kapadia,* University of Southern California*; Xinyu Bao,* Taiwan Semiconductor Manufacturing Company, Taiwan*; Jayakanth Ravichandran,* University of Southern California

Scaling of transistors has enabled continuous improvement in the performance of logic devices, especially with recent advances in materials engineering for transistors. However, there is a need to surpass the horizontal limitations in chip manufacturing and incorporate the vertical or third dimension. To enable monolithic three-dimensional (M3D) integration of high-performance logic, one needs to solve the fundamental challenge of low temperature (<450 °C) synthesis of high mobility n-type and p-type semiconductor thin films that can be utilized for fabrication of back-end-of-line (BEOL) compatible transistors.1 Transition metal oxides are promising n-type materials; however there is a lack of p-type materials that can meet the stringent synthesis conditions of BEOL manufacturing. Zinc sulfide (ZnS), a transparent wide band-gap semiconductor, has shown room temperature p-type conductivity when doped with copper2 and crystallizes below 400oC when grown by pulsed laser deposition (PLD).3 Here, we report growth of crystalline thin films of ZnS by PLD on a variety of amorphous and polycrystalline surfaces such as silicon nitride, (SixNy) thermal silicon dioxide, (SiO2), hafnium dioxide, (HfO2), yttrium oxide (Y2O3), platinum, sapphire (Al2O3), and titanium nitride (TiN). X-ray diffraction shows texturing of ZnS on all surfaces, including when ZnS is directly grown on HF buffered oxide etched silicon. Crystalline quality is investigated using grazing incidence wide angle X-ray scattering measurements. Surface and interface quality is measured using X-ray reflectivity and atomic force microscopy measurements. Electrical characterization of the ZnS films is done by J-V measurements of ZnS on platinum and metal-oxide-semiconductor capacitor (MOSCAP) measurements of ZnS on SiO2 on heavily doped silicon. The J-V measurements indicate low leakage current on the order of 10-8 A/cm-2 with electric field of 0.013 MV/cm2 and the MOSCAP characteristics show bilayer capacitor behavior, which points to ZnS being highly intrinsic with very low unintentional, electrically active point defects. Further work on doping ZnS with copper or other p-type candidate dopants are needed to demonstrate ZnS as a dopable wide band gap semiconductor for channels compatible with BEOL manufacturing. This work showcases the capability of novel thin film growth technique of a wide band-gap sulfide semiconductor in BEOL compatible conditions with potential for technological applications in transistor manufacturing.

1. S. Datta et al., IEEE Micro.39, 6, 8-15 (2019)

2.R. Woods-Robinson et al., Adv. Electron. Mater. 2, 1500396 (2016)

3. M. Surendran et al., Adv. Mater. 36, 2312620 (2024)

3:45pm **TF+CPS+MS+EM-ThA-7 Thermal Atomic Layer Deposition of Molybdenum Phosphide Films**, ***John Hues***, *Wesley Jen, Nolan Olaso, Steven M. Hues, Elton Graugnard,* Boise State University

Aggressive scaling of semiconductor technology nodes has led to copper-based interconnects beginning to approach the maximum scaling limit of the material, beyond which unacceptably high increases in interconnect resistance due to electron scattering at grain boundaries and interfaces begins to cause degradation of device performance. New materials are required for interconnect applications beyond the 7 nm node to produce devices with acceptable signal delay and power consumption parameters. Topological semimetals are one family of materials that are of interest for the replacement of copper in interconnect applications due to the predicted favorable resistance scaling, which results from topologically protected surface states that suppress electron scattering and act as conduction pathways in nanoscale films. This decrease in interconnect resistance has the potential to improve the efficiency of integrated circuits through reduced RC delay and reduced energy consumption, which is under increased scrutiny due to increasing computing demands, such as generative artificial intelligence and cloud computing. In order to aid in the integration of these promising materials into production environments, scalable synthesis methods, such as atomic layer deposition (ALD), are needed. In addition to the development of deposition chemistries for these materials, insight into how processing conditions impact the performance of the resulting film are also of importance. Here, we report on a new thermal ALD deposition chemistry for molybdenum phosphide (MoP) using molybdenum(V) chloride ($MoCl_5$) and tris(dimethylamino)phosphine (TDMAP) at temperatures between 350 °C and 425 °C. In-situ and ex-situ characterization of the resulting films was performed using quartz crystal microbalance (QCM), x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD), atomic force microscopy (AFM), scanning electron microscopy (SEM), and four-point probe measurements. QCM measurements demonstrated a linear mass increase of 164 ng/cycle at 375 °C. Film deposition was confirmed through XRD and XPS chemical state analysis. The resulting films were near stoichiometric as determined via XPS. AFM and SEM characterization revealed a polycrystalline morphology with nanoscale grain sizes. Four-point probe measurements of the as-deposited films indicated non-ideal electrical performance which was subsequently improved through post deposition annealing. Although more work is needed to improve electrical performance, this new ALD chemistry may provide a method for the deposition of MoP films at the dimensions required for next generation technology nodes.

4:00pm **TF+CPS+MS+EM-ThA-8 Wafer-Scale MgB_2 Thin Films: Fabrication, Characterization, and Device Development**, ***Jonathan Greenfield***, *Philip Mauskopf,* Arizona State University*; Clifford Frez, Daniel Cunnane,* Jet Propulsion Laboratory (NASA/JPL)

We report our work on wafer-scale MgB_2 thin films and devices. By optimizing the sputtering conditions, including precise control of the RF power, substrate bias, and a boron capping layerwe achieve highly uniform thin films with a surface roughness below 0.5nm and a superconducting transition temperature (Tc) in the range of 28–35K. The process improvements not only yield excellent wafer uniformity and scalability, but also overcome challenges previously associated with reactive evaporation and high-temperature oxidation. Building on these fabrication milestones, we have fabricated coplanar waveguide (CPW) resonators to investigate the fundamental microwave properties of MgB_2 thin films at 4.2K. Measurements of the kinetic inductance reveal values around 5.5pH/□ for 40 nm films, which are comparable to those of widely used high kinetic inductance materials. Importantly, our studies show a strong nonlinear kinetic inductance response under DC bias. By analyzing the phase delay in our transmission lines and resonators as a function of applied current, we extract a characteristic non-linear current parameter (I*), with corresponding current density values in the range of 12–22MA/cm^2. The high ratio of critical current to I* (~0.22) underscores the significant nonlinearity inherent in these films which is critical for the operation of superconducting parametric amplifiers and other microwave devices. Further extending the applicability of our MgB_2 thin films, we have integrated these materials into device architectures beyond passive resonators. Collectively, the evolution of our process from the initial demonstration of sputtered, wafer-scale MgB_2 thin films to the detailed characterization of their nonlinear kinetic inductance properties establishes a versatile platform for advanced superconducting device fabrication. The integration of phase shifters, frequency multipliers, parametric amplifiers, and thermal kinetic inductance detectors (TKIDs) further broadens the potential applications of these films in next-generation superconducting circuits, where high operation temperatures and broad frequency ranges are essential. Looking ahead, continued optimization of deposition parameters, stoichiometry control, and device integration strategies will be crucial in pushing the performance envelope and achieving robust, scalable thin film devices for both microwave and quantum applications.

4:15pm **TF+CPS+MS+EM-ThA-9 Selective Dry Etching of Boron-Doped SiGe Layers Using CF_4-Based Chemistry for 3D-Stacked Devices**, ***Jihye Kim***, *Joosung Kang, Dongmin Yoon, Dae-Hong Ko,* Yonsei University, Korea

With conventional scaling reaching its physical limits, vertically stacked device architectures—such as three-dimensional dynamic random-access memory (3D-DRAM) or complementary field effect transistors (CFETs)—have been proposed, necessitating enhanced fabrication approaches for their realization. One promising strategy involves the use of boron-doped SiGe/Si multilayer structures, where boron doping mitigates strain and facilitates the formation of defect-free, highly stacked structures. In this

scheme, the boron-doped SiGe layers serve as sacrificial materials, and their selective and uniform removal without damaging the Si layers is essential for precise Si channel formation. CF_4-based dry etching is widely employed for SiGe materials due to its high etch efficiency with conventional plasma processes. However, boron doping can significantly alter SiGe etching behavior by modifying the bonding structure, oxidation tendency, and volatility of reaction byproducts, highlighting the need to understand its effects under CF_4 plasma conditions.

In this study, we investigate the dry etching characteristics of boron-doped SiGe layers using inductively coupled plasma with CF_4-based gas chemistry. Etch rate variations were examined with respect to boron doping concentration in both single-layer and multilayer structures. Changes in surface roughness and chemical composition before and after etching were analyzed using atomic force microscopy and X-ray photoelectron spectroscopy to assess etch-induced surface modifications. These results provide insights into the etch mechanism and contribute to the optimization of selective etching processes in next-generation 3D-stacked device fabrication.

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