## Plasma Science and Technology
## Room 201 ABCD W - Session PS1-TuA

### Plasmas in Advanced Packaging

**Moderators: Catherine Labelle**, Intel Corporation, **Eric Miller**, IBM

2:15pm **PS1-TuA-1 Critical Plasma Processing Steps for Fusion and Hybrid Bonding Applications**, ***James Papanu***, Tokyo Electron Corporate Innovation Division / Tokyo Electron Kyushu, Ltd., Japan; *Scott Lefevre, Jeffrey Shearer,* TEL Technology Center America; *Michiko Nakaya,* Tokyo Electron Corporate Innovation Division, Japan; *Yousuke Mine, Yutaka Yamasaki,* Tokyo Electron Kyushu, Ltd., Japan; *Takayuki Ishii,* Tokyo Electron Kyushu, Ltd, Japan; *Christopher Netzband,* TEL Technology Center America; *Yuji Mimura,* Tokyo Electron Kyushu, Ltd., Japan; *Chikashi Aoyagi,* Tokyo Electron Ltd., Japan; *Ilseok Son, Angelique Raley, Sitaram Arkalgud,* TEL Technology Center America **INVITED**

Die-to-wafer (D2W) and wafer-to-wafer (W2W) hybrid and fusion bonding are integral to advanced packaging applications. Prior to bonding, for both D2W and W2W approaches, surface preparation is performed to facilitate the bonding process. Surface preparation consists of plasma activation and wet cleaning and hydration process steps. These steps are critical to obtain good interface quality and in turn high yield bonding that is void-free with high bond strength. Plasma surface activation is typically a relatively short, low power process. Nonetheless, the plasma source hardware and process conditions must be optimized to provide sufficient activation without roughening the dielectric layer (fusion and hybrid bonding) or sputtering and/or heavily oxidizing the bond pad Cu (hybrid bonding).

D2W bonding is required for chiplet heterogenous integration, and also offers the potential for yield improvement by the use of known good die for high bandwidth memory (HBM) and CMOS image sensor (CIS) applications. For D2W bonding, singulated die are bonded directly onto the target wafers. However, the quality of the die singulation process directly impacts the bonding yield. Defectivity levels for traditional saw dicing are too high for high volume D2W manufacturing. As such, advanced singulation techniques, such as plasma dicing are an essential part of the D2W ecosystem. For plasma dicing, there are two approaches, referred to as dice before grind (DBG) and dice after grind (DAG). For DBG, the etching process is performed before wafer thinning. The etching process trenches or grooves the full thickness wafers, and the dies are then singulated during the backgrind thinning process. For DAG, the etching process directly singulates or dices the thinned wafer, landing on a carrier. Consequently, the DBG and DAG have different process requirements and integration challenges.

In this paper, an overview of the fundamental mechanisms, chamber hardware factors, key process parameters, and process integration considerations for surface activation and plasma dicing steps will be presented. In addition, implementation of surface activation plasma for onto bonding cluster tools will be discussed.

2:45pm **PS1-TuA-3 Plasma processing opportunities in the era of Chiplet and Advanced Packaging for AI application**, ***Fee Li Lie***, *Shravana Kumar Katakam, Yann Mignot, Eric Perfecto,* IBM Research Division, Albany, NY **INVITED**

The evolution of artificial intelligence (AI) and machine learning (ML) technologies has exponentially accelerated the computing and memory power needed to train AI systems. This leads to larger and larger System on Chip (SoC) dies, some of which are hitting the lithography reticle limit or experiencing area-driven reduction of die yield. There is an additional need for very high bandwidth between processors and large arrays of memory. One emerging solution is to disaggregate large SoC dies into chiplets and re-connect them using advanced packaging techniques. Interconnection between chiplets can occur directly on the package substrate (“2D”), on an interposer (“2.xD”), through stacking of multiple chiplets (“3D”), or potentially a combination of these different technologies depending on application requirements. Die to die interconnect bandwidth and latency are key and we can broadly categorize these connections as lateral or vertical. Lateral interconnection is usually achieved through dual damascene Cu wiring in hard dielectric or plated-up Cu wiring in organic dielectric. Vertical interconnection is usually achieved by using “through” vias, namely Through Silicon Via (TSV), Through Dielectric Via (TDV), or Through Mold Via (TMV), in conjunction with fine pitch micro bump or Hybrid bonding for die to die joining. In this talk, we will discuss plasma processing opportunities in the era of Chiplet and Advanced Packaging, with emphasis on 3D integration with active Si interposers. We will introduce an overview of plasma processes typically used in 3D integration, and then review scope of needed improvements for some of the critical processes such as TSV RIE, Si thinning, and TSV reveal. Finally, emerging plasma applications for hybrid bonding such as plasma dicing will be introduced.

3:15pm **PS1-TuA-5 Characterization of Atmospheric Plasma Activation of GaAs Surfaces for Advanced Packaging**, ***Sarah Robinson***, *Karthik Sridhara, Kristen Steffens,* National Institute of Standards and Technology (NIST); *Junyeob Song,* National Institute of Standards and Technology (NIST)/ Theiss Research; *Andrew Winchester, Richard Allen, Daniel Schmidt, Sujitra Pookpanratana, Marcelo Davanco,* National Institute of Standards and Technology (NIST)

With the incorporation of heterogenous materials, such as GaAs and InP, on silicon substrates, surface treatments and preparation of the III-V surfaces have been demonstrated to be essential to lower temperature processing required for direct bonding of heterogenous materials. Atmospheric plasma systems flow a carrier and reactive gasses in tandem through an internal plasma zone producing a combination of high-energy charged particles and lower energy neutral radicals [1]. Due to the distance from the plasma zone to the substrate surface, the majority of the high-energy, charged particles have recombined and thus the remaining reactive species to reach the substrate surface contain low-energy, neutral radicals that can activate the surface without significant ion bombardment [1]. We are investigating the surface chemistries present after activation with atmospheric plasmas and performing bond strength measurements to provide key data to potentially optimize an empirical approach of many process development efforts.

In this study we are exploring the parameter space for different plasma types to observe variations in the surface chemistry of GaAs surfaces. We employ x-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM) to understand the physical and chemical changes with different surface treatments and plan to perform correlative bond strength measurements. We initially have studied the effect of nitrogen and oxygen based atmospheric plasmas on the native oxide of GaAs. XPS compositional analysis has shown the increase of both $As_2O_3$ and $As_2O_5$ with oxygen plasma treatment and primarily an increase of $As_2O_3$ with nitrogen plasma treatment. Additionally, AFM is used to ascertain roughness effects of atmospheric plasma treatments. Through process development we are varying the plasma chemistries, duration, and time dependance in conjunction with bonding to oxidized silicon substrates. We are currently working on improved methods to measure bond strengths and are developing test structures. The goal of our collaborative efforts is to combine a detailed surface science understanding with bond strength measurements as well as providing key process related conditions that can be broadly shared.

Acknowledgement: This work was performed with funding from the CHIPS Metrology Program, part of CHIPS for America, National Institute of Standards and Technology, U.S. Department of Commerce.

[1] E.F. Schulte, K.A. Cooper, M. Phillips, S.L. Shinde, IEEE 62nd Electronic Components and Technology Conference. San Diego, CA, USA **2012**, 26–30 (2012).

4:00pm **PS1-TuA-8 XPS Analysis of Surfaces and Interfaces for Improved Chip Bonding**, ***Kristen Steffens***, *Sarah Robinson,* National Institute of Standards and Technology (NIST); *Junyeob Song,* Theiss Research; *Karthik Sridhara, Berc Kalanyan, Sujitra Pookpanratana, Daniel Schmidt, Marcelo Davanco,* National Institute of Standards and Technology (NIST)

Bonding plays an important role in advanced microelectronics integration and packaging by bringing together components and devices fabricated separately.In addition to other important factors, surface-pretreatments on materials including metals, dielectrics and III-V’s have been consistently found to be crucial to achieving a high-quality bond, despite incomplete understanding of why certain treatments have greater success than others.Our project aims to improve understanding of some of these bonding pre-treatment effects to help enable more efficient development of bonding protocols, focusing on materials relevant for photonic and electronic devices.

Bonding of III-V semiconductors onto silicon enables fabrication of heterogeneous integrated photonic devices featuring low-loss waveguides and optical gain.[1]$Al_2O_3$ grown by atomic layer deposition (ALD) constitutes an effective intermediate layer between III-V’s and $SiO_2$, as $Al_2O_3$ films can achieve a higher interface energy even with low temperature annealing.[1,2]We have used x-ray photoelectron spectroscopy (XPS) to characterize GaAs surfaces prior to and post common ‘preps’ as well as

after plasma or thermal ALD of sub-6 nm $Al_2O_3$ layers.Such thin films allow observation of both the 3d and 2p regions for Ga and As, giving insight into chemistry at different depths of the material, including the interface.Results provide insight into surface prep effects and support previous reports that thermal ALD removes native GaAs oxides.

Regarding electronic devices, plasma-pretreatments can promote better bonding of important contact metals such as In, which is used in e.g. cryo-cooled detectors.Preliminary results show $He/H_2/N_2$ atmospheric plasma treatments increase $InO_x$ with little change to the metal signal and suggest that plasma-treated In displays a lower surface work function as compared to a control.We plan to extend our studies to include Cu, a critical material for hybrid bonding applications, and also to investigate plasma surface treatments via an in-situ remote plasma source on the XPS without atmospheric exposure.We anticipate that these results will add valuable insight into various bonding chemistries and their relation to bond strength or efficacy to help improve bonding process development in the future.

Acknowledgement: This work was performed with funding from the CHIPS Metrology Program, part of CHIPS for America, National Institute of Standards and Technology, U.S. Department of Commerce.

[1] H.K. Sahoo, L. Ottaviano, Y. Zheng, O. Hansen, K. Yvind, J. Vac. Sci. Technol. B 36(1) (2018) 011202-1 to 6.

[2] T. Gougousi, *Prog. in Crystal Growth and Char. of Mat.* **62** (2016) 1-21.

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