Plasma Science and Technology
Room 201 ABCD W - Session PS-MoM

Advanced Logic and EUV Patterning

Moderators: John Arnold, IBM, **Angelique Raley**, TEL Technology Center, America, LLC

8:15am **PS-MoM-1 Current Status and Future Perspectives of Plasma-Induced Damage and its Characterization**, ***Koji Eriguchi***, Kyoto University, Japan **INVITED**

Defect generation during plasma processes (plasma-induced damage, PID) is a crucial challenge in electronic device design. Various techniques, including atomic layer etching and cryogenic processing, are believed to control PID. To ensure low PID, precise characterizations and a deeper understanding of the fundamental physics behind experimental observations are indispensable. This study reports recent progress in PID characterization and discusses the fundamental aspects as future perspectives.

PID is now evaluated by electrical methods [1]. With the introduction of low-*k* films, mechanical property changes by PID have become another focus. Recently, a cyclic nanoindentation (c-NI) method [2] revealed that SiN films degrade more significantly than SiO_2 films by PID, particularly in terms of contact stiffness evolution. Mechanical property changes by PID should be considered for various applications.

Impedance spectroscopy (IS) was proposed to assess various aspects of PID in SiN and SiO_2 films [3]. An IS-based method was applied to Si and InP [4], one of the promising compound semiconductors for next-generation devices. Capacitive and conductive components were found to depend on the incident species from plasma. The IS-based method identified differences in the energy profiles of defects created in Si and InP substrates.

PID is governed by indeterministic dynamics. Molecular dynamics simulations [5] revealed that PID is formed by stochastic straggling within the sidewalls of "fin" structures. An increase in junction current (~dark current in CMOS image sensors) was experimentally confirmed using device arrays [6], highlighting the need to incorporate stochastic mechanisms in designing plasma processes for 3D and ultimately scaled devices. Recently, the stochastic aspects of PID were modeled similarly to stock price predictions, revealing Poisson statistics in defect creation and fundamental PID variation [7].

PID is inherently unavoidable. A deeper understanding and advanced characterization techniques are indispensable. This study reports mechanical property degradation and new characterization methods. Stochastic mechanisms in 3D and ultimately scaled devices have been discussed. Exploring various techniques and predictive models will be essential for future PID design.

[1] K. Eriguchi, Jpn. J. Appl. Phys. **60**, 040101 (2021).

[2] T. Goya *et al*., J. Phys. D **57**, 475202 (2024).

[3] T. Kuyama *et al*., IEEE IRPS, 4B.4 (2021).

[4] T. Goya *et al*., Jpn. J. Appl. Phys. **63**, 06SP04 (2024).

[5] K. Eriguchi *et al*., Jpn. J. Appl. Phys. **53**, 03DE02 (2014).

[6] Y. Sato *et al*., J. Vac. Sci. Technol. B **40**, 062209 (2022).

[7] K. Eriguchi and K. Urabe, Dry Process Symp., 17 (2023).

8:45am **PS-MoM-3 Direct Etching of Ru Pattern with Space Width of 10 nm and Less**, ***Miyako Matsui***, Hitachi, Ltd., Japan*; Kiyohiko Sato, Makoto Miura, Kenichi Kuwahara,* Hitachi High-Tech Corp., Japan

With continuous device scaling, scaling of the metal pitch is continuously required using advanced patterning technologies such as extreme ultraviolet lithography. As such scaling continues, alternative metal interconnects are required to replace Cu. Ru is a candidate for an alternative interconnect material with metal pitches of 20 nm and beyond because a Ru interconnect can have a lower effective resistance than that of a Cu interconnect at such small pitches. Ru can be etched directly, which can lead to new scaling boosters such as semi-damascene patterning. In the Ru etching process, roughness or other damage should be suppressed to reduce interconnect resistance.

In our previous study, we investigated the mechanism generating roughness in Ru patterns with a 32-nm pitch by using Cl_2/O_2-based plasma generated by a microwave-ECR etching system. The Ru sidewall roughness was thought to be caused by non-volatile RuO_x and $RuCl_y$, which were non-uniformly formed on the Ru sidewall. We found that the sidewall roughness of a Ru pattern strongly depends on the protection layers formed on the sidewall by adding passivation gas to the Cl_2/O_2-based plasma.

In this study, we investigated the etching mechanism of Ru patterns with a space width of 10 nm or less. The effect of space width on the etching performance and cross-sectional profiles of Ru patterns with a narrow space width was investigated. The space width of a Si_3N_4 mask pattern with a width of 14 nm was narrowed using an in-situ atomic-level deposition technique, which almost conformally deposited an atomic-level-thick SiO_2 layer on a Si_3N_4 mask pattern with a 32-nm pitch.

Etch stop occurred on the patterns when the space width of the mask pattern was narrower than 9 nm because the SiO_2/Si_3N_4 hard mask widened due to the redeposition of Si-containing by-products, and the redeposited by-products prevented ions from entering the space. When the ion energy was increased by applying a higher wafer bias power and the ion flux decreased by reducing the duty cycle of the wafer bias, Ru etching proceeded, but the Ru sidewall was laterally etched by radicals during the off-period of the wafer bias power. Ru sidewall protection becomes more important in preventing the lateral etching of Ru patterns with a narrow space because the ratio of radical to ion flux becomes large inside the narrow space.

We suggest adding a passivation gas to the Cl_2/O_2 plasma to form a protection layer on the sidewall of patterns with a space width of 10 nm or less. Sidewall roughness was also reduced because the Ru sidewall was protected from the etching by a uniform protection layer.

9:00am **PS-MoM-4 Study of Electron-Surface Interactions for Etching of Ruthenium with Chlorine and Oxygen**, ***Michael Hinshelwood***, University of Maryland College Park*; Hubertus Marbach, Michael Remmel, Gerson Mette, Michael Budach, Daniel Rhinow, Klaus Edinger,* Carl Zeiss SMT GmbH, Germany*; Gottlieb S. Oehrlein,* University of Maryland College Park

Ruthenium (Ru), a material used in semiconductor manufacturing for extreme ultraviolet (EUV) photomasks, is experiencing increasing attention as a material for capping layer and as potential adsorber in high NA lithography. Ru can be etched through the formation of volatile oxides and considerable research efforts have been put into optimizing etching processes. Y. Li et al. demonstrated that Ru can be rapidly etched by combining a low-energy electron beam (EB) with a flux of O_2/Cl_2-derived neutrals emanating from a remote plasma (RP) source [1]. This etching demonstrated a synergistic effect, with the remote plasma by itself causing a low level of etching, and the combination of EB and unexcited gas resulting in growth of a non-volatile compound. Here, we build upon that work, using in-situ ellipsometry to gain understanding on how the EB affects the surface etching reaction. By breaking up the exposure steps, subjecting the Ru surface to sequential EB and RP with either Cl_2 or O_2, we have found that the EB in conjunction with Cl_2 gas induces the uptake of Cl on the Ru surface, creating a chlorinated layer. The growth rate of this layer increases with increasing electron flux and energy, suggesting that electron-induced modification of the Ru surface is the source of the observed behavior. This chlorinated layer is selectively etched by O_2 plasma-derived neutrals, which otherwise results in non-volatile RuO_2 growth on the unmodified Ru. The etch rate of this modified layer increases with layer thickness, and is boosted by electron flux, suggesting that the electrons have multiple roles in this etching system. By isolating the effects of the EB on this etch mechanism of Ru, we obtained valuable information for the development of low-damage etch processes. Ellipsometric data and models of surface processes are complemented by X-ray photoelectron spectroscopy data.

This material is based upon work supported by Carl Zeiss SMT GmbH.

[1] Y. Li *et al.*, "Investigation of ruthenium etching induced by electron beam irradiation and O2/Cl2 remote plasma-based neutral fluxes: Mechanistic insights and etching model," *J. Vac. Sci. Technol. A*, vol. 43, no. 2, p. 023005, Feb. 2025, doi: 10.1116/6.0004219.

9:15am **PS-MoM-5 Challenges and Perspectives in Process Control for Next Generation Devices**, ***Cedric Thomas***, Tokyo Electron America, Inc.*; Yusuke Takino, Takehisa Saito, Naoki Fujiwara,* Tokyo Electron Miyagi Limited, Japan*; Tsung-Chen Lin, Shyam Sridhar,* Tokyo Electron America, Inc. **INVITED**

The scaling of logic devices is driven by the formation of three-dimensional structures for which atomic level control becomes mandatory. As Gate-All-Around (GAA) FETs are being developed for the production of advanced nodes, the needs for precisely controlled processes are increasing exponentially.

Time modulation (pulsing) of plasma parameters and species has become a widely adopted technique in the industry. Pulsed plasma is known to mitigate plasma-induced damage, enable unique chemical reactions, and produce distinct combinations of reactant fluxes and ion energies. Recently, there has been a resurgence of interest in plasma pulsing operations due to the availability of more complex pulsing schemes. However, with the increasing complexity of these schemes, there is a heightened need for advanced sensing and control systems.

In this talk, we will review the current status of plasma pulsing in process engineering and its applications. We will then discuss the requirements for complex pulsing schemes and control systems, and finally, we will share future prospects in this field.

9:45am **PS-MoM-7 Highly Selective Isotropic etching of SiGe over Si via Pulsed RF Power in NF_3 Plasma**, *Geun Young Yeom,* ***Hong Seong Gil****, Woo Chang Park, Yun Jong Jang,* Sungkyunkwan University (SKKU), Republic of Korea

Highly selective isotropic dry etching of SiGe for Si is an important process for fabricating 3D-structured GAA-FETs or 3D DRAM. Si-Ge bonds, which are relatively weaker than Si-Si bonds, are more easily fluorinated by F-radicals and thus are etched as SiF_4 and GeF_4. However, because the high reactivity of fluorine radicals makes it challenging to achieve damage-free SiGe etching using F-radical-based approach, there is a growing demand for the development of more highly selective etch processes.

In this study, we employed an ICP-type remote plasma with NF_3 gas to investigate how pulsed RF power can be used to control the etch species and thereby to improve etch characteristics in isotropic SiGe etching. By applying microsecond-scale on/off cycles to the RF power, we found that the etch rate of SiGe maintained (or increased) while that of Si decreased, significantly enhancing the overall etch selectivity. Additionally, we found that lower processing temperatures significantly enhanced the etch selectivity, primarily due to differences in activation energies between Si and SiGe under pulsed plasma conditions.

10:00am **PS-MoM-8 Extreme Etch Selectivity of SiN/SiO_2 in CF_4 Plasma with a DC-biased Grid for High Precision GAAFET Etching**, ***Minseok Kim****, Hyunho Nahm, Yujin Yeo,* Wangshipri ro 222 Hanyang university Engineering center 403-2, Republic of Korea*; Chinwook Chung,* Wangshipri ro 222 Hanyang university Engineering center 403-1, Republic of Korea

We present a method for enhancing selective etching in GAAFET fabrication by controlling CF_2 radical generation in an inductively coupled plasma (ICP) system equipped with a DC-biased grid. Modulating the grid voltage enables energy control of electrons passing through the grid, thereby influencing the dissociation dynamics of CF_4 gas. A negative bias accelerates electrons to higher energies, which enhances CF_2 radical production. Notably, when the grid voltage is reduced below –15 V, the CF_2-to-F radical ratio increases by approximately 30% compared to the unbiased condition. This behavior is attributed to the electron energy approaching the dissociation threshold of CF_2 (~15 eV) and the formation of an ultra-low electron temperature (ULET) plasma that helps preserve CF_2 radicals. The increased CF_2/F ratio contributes to the deposition of a fluorocarbon-based polymer layer on silicon surfaces, which promotes etching selectivity. As a result, the etch rate of Si is suppressed by about 40%, while that of SiO_2 increases by 30%, significantly improving the Si/SiO_2 etch selectivity. These results underscore the potential of electron energy control via DC grid biasing to tailor radical chemistry and enable advanced, selective plasma processing for next-generation device fabrication.

10:30am **PS-MoM-10 Influence of Nitrogen on Controlling the Etch Selectivity between Tungsten Metal and Dielectric Materials**, ***Indroneil Roy****, Pingshan Luan, Jason Marion, Yusuke Yoshida, Peter Biolsi,* TEL Technology Center America

Metal gate cut (MGC) last approach has many advantages over traditional poly gate cut such as increased separation length of the gate, improved composite yield, and lower parasitic leakage. In future device structures (e.g. Complementary Field Effect Transistor, CFET), the increase of gate heights along with the decrease of critical dimensions (CD) results in high trench aspect ratios (A.R., calculated by height/CD). This poses a significant etch challenge where the metal etch rate slows down and the etch profile becomes more difficult to control. Simply etching for longer may not be suitable because the hard mask, typically comprised of dielectric materials, will be fully consumed. Thus, a process that provides higher metal-to-dielectric selectivity is highly desirable for MGC applications. In this work, we use blanket films of tungsten (W), which is a typical metal gate material, and SiO_2 and Si_3N_4, which are typical hard mask materials, to investigate the effect of plasma chemistry in controlling etch selectivity. Particularly, the role of N_2 in a BCl_3/N_2 plasma is explored. We found that the W:SiO_2 and W:Si_3N_4 etch selectivity is governed by the interplay between etchant Cl neutrals, and a passivation effect when N_2 is introduced in the plasma. The etch amounts of W, Si_3N_4, and SiO_2 were evaluated using spectroscopic ellipsometry (SE). We found that the W etch amount (E.A.) increases with increasing N_2 flow whereas the dielectric E.A. decreases. However, in a low N_2 flow regime, the Si_3N_4:SiO_2 selectivity reverses. The behavior of N2 flow on etch selectivity was evaluated by studying the surface composition of these materials before and after etch using X-ray photoelectron spectroscopy (XPS). The effect of A.R. on etch selectivity was also investigated. The plasma composition is also monitored using optical emission spectroscopy (OES) to understand differences in relative concentration of gas phase species.

10:45am **PS-MoM-11 Plasma Etch of Low-K Dielectric (SiOC, SiOCN) at Reduced Temperature**, ***Sang-Jin Chung****,* University of Maryland, College Park*; Pingshan Luan, Adam Pranda, Yusuke Yoshida,* TEL Technology Center America*; Gottlieb Oehrlein,* University of Maryland, College Park

Front-end low-k dielectric (SiOC, SiOCN) are important in complementary field-effect transistors (CFET) for reducing LC delay, minimizing power consumption, and mitigating crosstalk. Future generations of CFETs will also be increasingly stacked to improve device density. Therefore, high-aspect-ratio (HAR) etch and profile defect issues must be considered, as well as the different etch rates of the dielectric/poly-Si materials which will be dependent on the precursor chemistry, substrate temperature, and plasma power.

In this work using an inductively coupled plasma chamber, we will examine SiOC and SiOCN etch both isotropically and anisotropically with varied substrate temperatures (10 °C to -60 °C), precursors, plasma power, and bias voltages. *In situ* ellipsometry will be used to monitor the real time etch behavior, and XPS will be used to probe the composition after etching.

The etch capability of the chamber at cryogenic temperatures has been successfully confirmed.[1] In this work, *in situ* ellipsometry monitoring of the surface can give us a powerful understanding of the chemical properties of the deposited FC film when etching SiOC and SiOCN material, particularly as we lower the substrate temperature when condensation might occur.

In addition to planar etch of these substrates, HAR structures will be used to simulate isotropic etch characteristics of the SiOC and SiOCNmaterials. A previous study using Si_3N_4 and SiO_2HAR structures showed significant spontaneousetch when using HFC precursors (CH_2F_2, CHF_3, and CF_4/H_2) whereas mostly deposition was seen with FC precursors (C_4F_8).[2] Our current results show that at low substrate temperature, this isotropic etch was mitigated. The etching characteristic and sidewall profiles of SiOC and SiOCN materials will be compared to SiO_2 and Si_3N_4.

1. Kihara, Y., Tomura, M., Sakamoto, W., Honda, M. & Kojima, M. Beyond 10 µm depth ultra-high speed etch process with 84% lower carbon footprint for memory channel hole of 3D NAND flash over 400 layers. 2023 IEEE Symposium on VLSI Technology and Circuits, 1–2 (2023).
2. Chung, S.-J., Luan, P., Park, M., Metz, A., & Oehrlein, G. S. Exploring oxide-nitride-oxide scalloping behavior with small gap structure and chemical analysis after fluorocarbon or hydrofluorocarbon plasma processing. J. Vac. Sci. Technol. B 41, 062201 (2023).

11:00am **PS-MoM-12 Etch Characteristics of Flexible Low-*k* SiCOH Thin Films Under Fluorocarbon-Based Plasmas Using Inductively Coupled Plasma-Reactive Ion Etching Process**, ***Rajib Chowdhury****, Thomas Poché, SeonHee Jang,* University of Louisiana at Lafayette

Flexible electronics have gained considerable attention within the microelectronics industry due to their ability to fold, twist, stretch, and conform to various surfaces. Unlike traditional Si-based electronics, flexible electronic devices are fabricated on substrates such as polymers, metal foils, and flexible glass, enabling applications in displays, wearable devices, and solar cells. However, low-temperature processing is required to produce flexible electronic components due to the low glass transition temperature of polymer substrates. Among various dielectric materials, carbon-doped silicon oxide (SiCOH) is widely used in semiconductor devices for its low dielectric constant (low-*k*, $k < 4.0$). Photolithography and dry etching are essential for integrating SiCOH into flexible electronics. While the etching properties of SiCOH films on rigid Si wafers are well-studied, research on flexible SiCOH films is limited. In the dry etching process, etchants such as CF_4, O_2, and Ar influence the film properties, potentially affecting device performance. This study explores the effect of etching

parameters on flexible SiCOH films to advance their application in flexible electronics.

Flexible low-*k* SiCOH films were produced onto flexible indium tin oxide-coated polyethylene naphthalate substrates by plasma-enhanced chemical vapor deposition of a tetrakis (trimethylsilyloxy)silane precursor at ambient temperature. RF plasma powers of 20 and 60 W were utilized for the deposition. An inductively coupled plasma-reactive ion etching process was performed to investigate the etching characteristics of the SiCOH films under CF_4-based plasmas. Each etching gas chemistry was selected among CF_4, $CF_4 + O_2$, and CF_4 + Ar. The physical, chemical, and electrical properties of the SiCOH films were investigated to determine the effects of etching process parameters on film's properties.

The Fourier transform infrared spectra of the pristine films identified four prominent absorption bands as CH_x stretching, $Si\text{-}CH_3$ bending, Si-O-Si stretching, and $Si\text{-}(CH_3)_x$ stretching vibration modes. After etching, the peak area ratio of Si-O-Si stretching mode increased, and that of $Si\text{-}(CH_3)_x$ stretching mode decreased. The high-resolution X-ray photoelectron spectroscopy scan found that the peak intensity of the C1s and Si2p peaks decreased after the etching process, and the peak center of the F1s peak shifted depending on etching chemistry. The *k*-values of the pristine SiCOH films deposited at 20 and 60 W were 2.46 and 2.00, respectively. Following etching, the *k*-values of the films at 20 W were reasonably consistent, while those at 60 W increased notably following the etching process.

11:15am **PS-MoM-13 Enhancing 24nm Pitch Line / Space by DSA Rectification: A Path to Smoother Lines and Car Extension**, ***Rémi Vallat***, *Lander Verstraete, Philippe Bézard, Hyo Seon Suh, Laurent Souriau, Kurt Ronse,* IMEC, Belgium

The introduction of extreme ultraviolet (EUV) lithography tools has significantly accelerated the scaling of device features, driving advancements in the semiconductor industry. However, as critical dimensions (CD) continue to shrink, the impact of stochastic variability becomes even more pronounced, and the demands for precise patterning grow stricter. Traditional chemically amplified resist (CAR) materials are facing increasing challenges in meeting specifications for roughness, defectivity, and etch budget. As a result, there is a rising interest in exploring alternative resist formulation and patterning schemes, such as directed self-assembly (DSA).

DSA can mitigate the stochastic issue and push EUV patterning close the resolution limit, thanks to its resilience to small resist variation by extending the use of CAR combined with low dose exposure. For DSA, PS-*b*-PMMA low chi block copolymer is typically used down to 22nm pitch, its phase separation limit. Scaling below 22nm requires the introduction of higher Chi materials to provide a sharper interface with less fluctuations and thus better roughness. [1-3]

In this talk, the case of rectification by DSA at Pitch 24nm Line/ Space CAR patterns (P24 L/S) will be discussed (Figure 1). After introducing the DSA process flow, we will present how to minimize the Line Edge Roughness (LER) and Line Width Roughness (LWR) by optimizing the stack and the dry etch pattern transfer process. Finally, we will discuss how to further improve the roughness (both LER and LWR) at BCP level (for both PS-*b*-PMMA and HighChi) and how the improved roughness is modulated during the pattern transfer down to the layer below.

[1] M. P. Stoykovich, K. C. Daoulas, M. Muller, H. Kang, J. J. de Pablo, P. F. Nealey, *Macromolecules*, 2010, 43, (5), 2334-2342.

[2] R. Ruiz, H. Kang, F. A. Detcheverry, E. Dobisz, D. S. Kercher, T. R. Albrecht, J. J. de Pablo, P. F. Nealey, *Science*, 2008, 321, (5891), 936-939.

[3] G. Singh, N. Nair, F. Gstrein, R. Schenker, Proc. SPIE PC12953, Optical and EUV nanolithography XXXVII, PC129530G, 2024.

11:30am **PS-MoM-14 Dry Etch Challenges Towards the High NA EUV Lithography Patterning Era**, ***Sara Paolillo***, *Stefan Decoster, Philippe Bezard, Remi Vallat, Vincent Renaud, Viktor Kampitakis, Annaelle Demaude, Laurent Souriau, Bhavishya Chowrira, Dieter Van Den Heuvel, Victor M. Blanco Carballo, Syamashree Roy, Shubhankar Das, Frederic Lazzarino,* IMEC, Belgium **INVITED**

Pitch scaling remains a fundamental driver of semiconductor technology advancement. To print smaller feature sizes, Extreme Ultraviolet (EUV) lithography was introduced starting from the 7 nm technology node. As we are approaching the scaling limits of Low Numerical Aperture (NA) EUV, High NA EUV lithography is being proposed as a solution for patterning sub-24 nm pitch structures in a single exposure step. Additionally, multi-patterning schemes are being employed to extend capabilities beyond the lithographic resolution limit. In all cases, to support this ongoing miniaturization, it is crucial to ensure the precise transfer of the photoresist patterns into underlying layers through plasma etching.

This presentation will highlight the opportunities and evolving challenges associated with dry etching at current resolutions and as we transition into the high NA era. As device features shrink, the lithography trade-off between resolution, sensitivity, and features roughness becomes increasingly challenging to balance; improving one comes at the expenses of the others. One major challenge is addressing local photoresist non-uniformities, such as height variations and residues after development, which can lead to defects (breaks or bridges) after pattern transfer. These effects become even more pronounced when using thinner resists required for High NA lithography. To mitigate these issue and improve pattern fidelity, strategies such as descum processes, enhanced etch selectivity, and novel break-healing techniques are being explored. Another key challenge related to the aforementioned trade-off is minimizing features roughness, including line roughness (LER/LWR), local CD non-uniformity (LCDU), and tip-to-tip (T2T) variability. We will discuss several methods to mitigate these effects, like directional etching, directed self-assembly, and precise tuning of etching parameters.

Beyond the challenges related to working at the limits of the lithographic process, patterning increasingly smaller features in the final stack also presents significant challenges. Achieving high selectivity, vertical profiles, minimal mask erosion, low feature roughness, and preventing line bending demands continuous advancement in both etching techniques and patterning stack design. We will discuss how the choice of materials within the stack and their properties affect patterning performance.

Finally, we will present case studies from IMEC where high NA exposure has been introduced, and we will discuss the results of pattern transfer.

Author Index

Bold page numbers indicate presenter