Manufacturing Science and Technology
Room Central Hall - Session MS-ThP

Manufacturing Science and Technology Poster Session

MS-ThP-1 Novel Inspection Technology for Detecting Via Open Using Parallel E-beam Scanning and Graphic Design System, ***Chihoon Lee***, SSIT (Samsung Institute of Technology), Republic of Korea

As dual-damascene Cu interconnect technique is currently being employed for on-chip interconnect fabrication, and will continue to be used for next technology generations due to significant cost advantage [1]. In this process, however, it has been challenging to detect via open defects occurring in the underlying layer after the completion of the Cu metal line. A viable in-line monitoring to detect via open defects in the back-end of line (BEOL) has been challenging due to the complex multiple via structures connected to the metal line. Today's conventional inspection method do not meet the requirements of a true in-line monitoring strategy [2]. Despite detecting the dark voltage contrast (DVC) signal as a via open defect in the conventional electron beam (E-beam) inspection system, it was not genuine defects in most cases by the transmission electron microscopy (TEM) analysis for detected via open defects. We guess that it is attributed to the complexity of the vertically designed BEOL metal/via structures, which makes it difficult to separate exact via open location in the upper and lower layers. Figure 1 shows exactly detected via open defect image and related metal/via layout with E-beam inspection system.Early in-line detection of these via open defects prior to the electrical die test is crucial for yield improvement. In this talk we demonstrate a novel inspection technology to detect the critical BEOL via open defects using parallel E-beam scanning and graphic design system (GDS). Parallel E-beam scanning is an inspection technique that can detect more electrons by adjusting the stay time of electrons according to the shape of the metal line pattern. It was controlled by the landing energy (LE), scan direction in the E-beam inspection system. In addition, the detecting locations of via open were restricted near single via layout using die to database (D2DB) inspection system to improve the detectability. It can effectively capture the signals of via open defects compared to the conventional E-beam inspection in the complex high dense metal/via structures.

[1] A. V. Vairagar et al., Appl. Phys. Lett. 87, 2005

[2] M. Daino et al., *28th Annual SEMI Advan. Semiconductor Manuf. Conference (ASMC)*, 2017

MS-ThP-2 EES2: Advancing Microelectronics and Computing Energy Efficiency Through a Co-Design Approach, ***I-Hsi Daniel Lu***, Energetics

The U.S. Department of Energy's (DOE) Energy Efficiency Scaling for Two Decades (EES2) initiative is a pioneering effort aimed at achieving a 1000x improvement in energy efficiency in all aspects of computing over the next two decades. This ambitious goal is based on the concept of doubling energy efficiency every two years—a new type of scaling—leading to a 1000x over two decades. EES2 focuses on operational efficiency in computing, —from hardware components to software elements.The roadmap leverages an integrated, interdisciplinary co-design approach to optimize energy use across the entire compute stack. Recognizing that the natural slowing of efficiency gains due to factors like the end of Dennard scaling challenge the industry, EES2 emphasizes the importance of co-design, where adjacent layers of hardware and software are developed in tandem to achieve energy efficiency by orders of magnitude without trading off performance.

The roadmap challenges the industry to achieve these ambitious efficiency goals, stimulating innovation and discussion by identifying key technologies that can serve as benchmarks. Through a series of near-, mid-, and long-term strategies, EES2 prioritizes energy efficiency in every aspect of design and development in Microelectronics. Central to this version 1.0 of the EES2 effort are eight working groups: Materials and Devices, Circuits and Architectures, Advanced Packaging and Heterogeneous Integration, Algorithms and Software, Power and Control Electronics, Metrology and Benchmarking, and Education and Workforce Development. These groups work collaboratively to ensure that the layers of the compute stack enhance energy efficiency, by using co-design as one of the approaches.

As EES2 expands its focus to include emerging technologies such as quantum computing and photonics, the initiative aims to return to or exceed the historical pace of energy efficiency enabled by Dennard scaling by innovations and set new benchmarks for the industry. This poster will explore the collaborative efforts among industry, academia, and national laboratories that underpin this initiative, emphasizing the transformative potential of the co-design approach in driving energy efficiency advancements in microelectronics.

Manufacturing Science and Technology
Room 117 - Session MS-FrM

Next Generation and Sustainable Micro-/Nano-Manufacturing

Moderators: Erica Douglas, Sandia National Laboratories, **Diane Hickey**, Department of Energy

8:15am **MS-FrM-1 DOE's Microelectronics Energy Efficiency Scaling for 2 Decades (EES2)***, **Tina Kaarsberg**,* U.S. Department of Energy*; J. Elam,* Argonne National Lab*; S. Misra,* Sandia National Laboratory*; S. Shankar,* SLAC National Accelerator Laboratory

In response to analysis showing both slowing efficiency improvements and exponential growth in electricity use by computing and other microelectronics technologies, the United States Department of Energy (DOE) Advanced Materials and Manufacturing Technology Office (AMMTO) is leading a multi-organization effort to counter these trends with its initiative in energy efficiency scaling for two decades (EES2) for microelectronics.Similar to the "scaling" of the first few decades of microelectronics, this energy efficiency scaling would result in the biennial doubling of integrated circuits' or chips' energy efficiency. DOE's EES2 initiative aims to flatten microelectronics energy by enabling 10 biennial efficiency doublings to more than a factor of 1000 in two decades. By Earth Day 2024, 65 organizations representing industry, academia, and DOE national laboratories had signed the EES2 pledge.A key element of the pledge is an EES2 R&D Roadmap to identify "technologies to beat" that are 10 to 10,000X more energy efficient that the technologies they would replace. Version 1.0 of the EES2 roadmap is focused on enabling energy efficiency in computing by software-driven co-design across all elements of the compute stack as well as continued innovation in new non-miniaturization-related device technologies and circuit architectures.This talk will present results of version 1.0 of the roadmap highlighted with EES2-sponsored R&D. This EES2 roadmap and the R&D inspired by it is the first phase of an ongoing commitment to energy-efficient and sustainable microelectronics electricity use incomputing, communications and other emerging applications. On August 14, DOE released the draft EES2 Roadmap [https://www.energy.gov/eere/ammto/articles/doe-seeks-input-dramatically-increase-energy-efficiency-semiconductor?utm_medium=email&utm_source=govdelivery] as part of an RFI [https://eere-exchange.energy.gov/Default.aspx] . The Roadmap itself is at EES2 Roadmap Version 1.0 focused on Compute [https://eere-exchange.energy.gov/FileContent.aspx?FileID=f4234e29-cc0c-4a56-a510-86b616ab5535] . Respond to the RFI by writing to micro.electronics@ee.doe.gov [mailto:micro.electronics@ee.doe.gov] .

8:30am **MS-FrM-2 An Energetically Low-Cost Future for Advanced Semiconductor Manufacturing***, J. Randall, **Joshua Ballard**,* Zyvex Labs

The DOE Advanced Materials and Manufacturing Technologies Office (AMMTO) sponsored Semiconductor Industry Energy Efficiency Scaling (EES2) roadmap has identified Extreme Ultraviolet Lithography (EUV) as a significant contributor to the energy budget of advanced digital electronics [reference roadmap and Bardon and Parvais 2023]. Strikingly, EUV is so inefficient that only about 0.04% of the beam energy actually affects the resist [Shankar 2023]. Additionally, EUV – and e-beam lithography (EBL) used to make masks for EUV–are reaching their resolution limits which limits the ability to continue to make operational efficiency gains in digital electronics typical with the march of Moore's Law and Dennard scaling which posits that energy consumption scales with total device or chip area. For conventional devices, the extra precision will also allow lower voltage swings for switching to be used, which will further reduce energy consumption during usage. In the particular case of quantum devices, extreme precision in their dimensions is required; a variation of 2 nm can halve or double tunnelling rates in a quantum dot qubit, a level of precision beyond the capability of EBL or EUV.

The EES2 roadmap identifies the replacement of EUV with Nanoimprint lithography (NIL) as a key takeaway. NIL offers equal and better resolution and precision than EUV, with up to 90% lower energy costs [DNP 2023], resulting in lower costs of production.

This presentation will describe a pathway towards unprecedented resolution in nanoimprint mask fabrication. Ultrahigh-precision NIL templates are made by writing sub-nm precision patterns on Si(001) using H Depassivation Lithography (HDL), followed by selective growth via atomic layer deposition (ALD) of a hard mask such as TiO_2, which is then used as an etch mask for Reactive Ion Etching (RIE) to form a 2.5D Si template, replicating the STM pattern. This template would then be transferred into a quartz template using existing step and flash NIL processes which will be used to pattern devices. We show that sub-10 nm feature sizes and full-pitch gratings with feature radius of curvature down to 1.5 nm in the lateral dimension can be achievable. This NIL therefore addresses two AMMTO goals; atomically-precise manufacturing, and the EES2 goal of improving the energy efficiency during manufacturing and–as a fortunate side effect–during operation of digital electronics.

8:45am **MS-FrM-3 Plasma Processing and the Semiconductor Supply Chain in an Era of Low GWP and/or PFAS-Free Gas Chemistries***, **Eric Joseph**,* IBM Research Division, T.J. Watson Research Center

Sustainability policy across the globe has become a major driver of change for the semiconductor industry and its supply chain.New net-zero emission goals and overall phase-out targets for PFAS materials are a noble cause, but an exemplary challenge to solve in a relatively short time.In this presentation, we will review the critical nature of PFAS and the widespread impact of these materials across the ecosystem.The evolution of fluorocarbon (FC) and hydrofluorocarbon (HFC) etch gas materials, a subset of PFAS which are essential in plasma processing applications, will be discussed in detail.The talk will then summarize ongoing and recent efforts to begin exploring (1) process optimization to minimize PFAS and high global-warming potential FC/HFC gas usage, (2) alternative low GWP or PFAS free material exploration and (3) capture/recovery/abatement opportunities to avoid release of these materials after use.The challenge throughout will be to satisfy all process metrics for success, which have been extensively researched over the past 50 years, and bring them towards full scale adoption industry wide which ultimately improves sustainability.

9:00am **MS-FrM-4 Patterning and Etch Development of High Aspect Ratio 2.5D MIM Capacitor Structures***, **Quyang Lin**, P. Nolmans, D. Montero Alvarez, F. Lazzarino, G. Beyer, G. Van der Plas, E. Beyne,* IMEC Belgium

The microelectronics industry demands smaller and more efficient chips for future-generation fabrication nodes. While most efforts of chip downscaling are focused on reducing the size of logic units, it is also important to scale capacitors accordingly to meet the design criteria of newer nodes. In this context, 2.5-D high-density metal-insulator-metal (MIM) capacitors (CAP) were proposed, offering several advantages such as high capacitance density, low parasitic impact, small form factor, and low cost [1][2]. Ref. [1] demonstrated 2.5-D MIMCAPs exhibiting 26nF/mm2 capacitance density, 3.6 times higher compared to 2D planar MIMCAP. In this work, we further scaled down 2.5-D MIMCAP by reducing the pitch, 70nF/mm2 is achieved with 10nm HfAlOx dielectric. Additionally, we pattern higher Aspect Ratio (AR) studs to effectively increase the capacitance density.

The initial design of 2.5-D MIMCAPs featured 1µm SiO2 studs with a 200nm Critical Dimension (CD) and 484nm pitch with a 5 AR [1]. Simulation results indicate that higher oxide stud enables higher capacitance density, with CD and pitch also crucial due to their role in defining the effective area and the thickness limitations of MIM layers. In this work, the development is conducted on 300mm wafers. 1-2µm oxides are deposited on top of a TaN layer. Then, the hard mask stack deposition process follows, composed of 50nm DARC and 1300nm APF. Immersion lithography is then employed to print studs with CD 200nm/Pitch 380nm. The pattern is transferred to the oxide layer, resulting in oxide studs up to 10 AR. MIMCAPs are then deposited on oxide studs (Supplement Fig. 1 and 2). Etch development becomes very challenging with such HAR and dense pitch due to the deterioration of studs: too small CD, excessive slope, and stud bending. Additionally, the thickness of APF is not supported to etch 2µm oxide, while the thicker APF is not the case because of wafer warping caused by compressive stress. To tackle these challenges, different etch investigations like gas mixture, high and low frequency powers have been conducted in various etch steps, to optimize the oxide stud CD and slope, and to understand their impact on the oxide etch rate and the selectivity to APF to enable oxide studs up to 2µm (Supplement Fig. 3 and 4).

In this work, new patterns of 2.5-D MIMCAPs are proposed, measured capacitance density is up to 70nF/mm2 on a 1µm oxide height. The formation of 2µm oxide studs of 200nm CD (10 AR) in a dense pitch of 380nm with ideal slope is ultimately achieved, promising a further substantial improvement on capacitance density. Moreover, this etch work shows the potential to achieve oxide studs with 15 AR.

9:15am **MS-FrM-5 CMOS Design Pathways to Sustainable Compute Scaling**, ***Azeez Bhavnagarwala,*** Metis Microsystems **INVITED**

In its Decadal Plan [1], the Semiconductor Research Corporation (SRC) projections of energy demand for computing versus global energy production are creating new risks - with semiconductors expected to consume nearly 25% of global energy by 2030. Computing power demands *double every two months* [2] where computational loads - in number of computations, continue to grow exponentially – driven primarily by the growth in artificial intelligence (AI) applications and training workloads. New approaches to computing, such as in-memory compute, special purpose compute engines, different AI platforms, brain inspired/neuromorphic computation etc. are identified by the SRC as necessary to support scaling of compute performance beyond barriers imposed by energy efficiency of conventional CMOS semiconductor architectures. In its Decadal Plan, the SRC asserts that *changing the computing trajectory with these innovations would be much more cost-effective than attempting to dramatically increase the world's energy supply*.

This work [3] describes alternative CMOS circuit architectures that harvest the evaluation energy of dynamic circuits - primarily used across CMOS memories and high performance CMOS arithmetic components while also engaging harvested charge to improve circuit speeds during signal development and data resolution. Harvesting circuits also self-regulate signal development by memory cells mostly eliminating the performance and energy overheads from bit cell variability seen with industry-typical circuit architectures enabling 10X improvements in the Energy-Delay metric at the component level - a 5X reduction in active energy without lowering operating voltages and a 2X improvement in circuit speed without raising operating voltages. Proposed circuit architectures do not require changes to the CMOS process, to the foundry bit cell or to the design, test and verification flows minimizing their risk and path to market. With over 70% of Accelerator chip power consumed by CMOS Memories [4], proposed circuit architectures also remove limitations on processor FMAX imposed by heat removal while also relaxing thermal constraints on the package design enabling higher semiconductor packaging efficiencies.

[1] https://www.src.org/about/decadal-plan/decadal-plan-full-report.pdf

[2] https://www.nature.com/articles/s41586-021-04362-w

[3] A Bhavnagarwala, published US Patents

[4] W Daly, Keynote at Hot Chips Conference 2023 https://hc2023.hotchips.org/assets/program/conference/day2/Keynote 2/Keynote-NVIDIA_Hardware-for-Deep-Learning.pdf [https://hc2023.hotchips.org/assets/program/conference/day2/Keynote%2 02/Keynote-NVIDIA_Hardware-for-Deep-Learning.pdf]

9:45am **MS-FrM-7 Semiconductor Technology Needs Vacuum - How Growth in the Semiconductor Industry and Sustainable Production Can Be Achieved**, ***Kevin Mahler,*** *K. Bergner,* VACOM, Germany

Everyone is talking about semiconductor manufacturing - but it is vacuum technology that makes it possible. In our presentation, we will highlight the role of vacuum technology as a high-tech enabler for essential key technologies in the field of semiconductor production. In particular, we will address the emerging tension between a projected market growth to $ 1 trillion in 2030, the necessary resource requirements and the increasing demands in the area of sustainability.

We then show how VACOM has implemented a sustainable vacuum mechanics production factory - far beyond the existing requirements from the semiconductor industry and politics. We highlight the role played by available resources such as air, water, sun, earth and people and how this is combined in a globally unique overall concept. The focus will be on sustainable infrastructure in production - a field of work that is sometimes underrepresented in product-related analyses and optimizations. In summary, we will show how ecological, economic and physiological possibilities can interact in a circular economy.

10:00am **MS-FrM-8 High Resolution Ion Beam Imaging, Nano-Scale Analytics and Nanofabrication with Light and Heavy Ions from a Single Ion Source**, ***Peter Gnauck,*** *T. Richter, A. Ost,* Raith GmbH, Germany

The liquid metal alloy ion source (LMAIS) technology has become a key component for Focused Ion Beams (FIB) nanofabrication in recent years [1]. Its remarkable beam current stability, patterning and imaging resolution, coupled with the ability to rapidly adjust the sputtering yield by switching between different ions within seconds, enable working on versatile applications using this source technology (Fig. 2).

The visualization of nanoscopic samples in 3D holds great significance across various domains, including nanotechnology, life sciences, and materials science, as it offers enhanced insights into surface and internal structures compared to traditional 2D imaging. While conventional methods for 3D volume reconstruction involve slice-wise imaging and milling of the sample with stage tilt, the usage of the LMAIS technology with light and heavy ions from a single source introduces a novel approach to obtain 3D volume information.

The GaBiLi source revolutionizes 3D imaging by alternating between imaging with Li^+ primary ions at high spatial resolution in secondary electron (SE) mode and fast switching to milling mode with Bi^+ primary ions with a high sputtering rate. Using this Mill&Image workflow the ion beam remains perpendicular to the sample surface without requiring sample tilt. The resulting collection of SE images can be assembled into a 3D stack, facilitating visualization of the sample's internal structures (Fig.1).

This FIB technology has been recently merged with a dedicated SIMS unit, combining high sensitivity, transmission and best spatial image resolution. The SIMS unit consists of key components like (i) specifically designed extractable/insertable secondary ion extraction and transfer optics ensuring maximum extraction efficiency and transmission, thereby ensuring high sensitivity, (ii) a compact floating double focusing magnetic sector mass spectrometer enabling operation in DC mode at high transmission, without performance-degrading duty cycles encountered in TOF systems, (iii) a continuous detector enabling the simultaneous detection of all masses in parallel.

This novel platform offers element imaging at the nanoscale, isotope differentiation, depth profiling and 3D chemical analysis (Fig. 3).

In this presentation, we will explore the potential for topographic 3D data with analytical surface information obtained through Secondary Ion Mass Spectrometry (SIMS), offering a forward-looking perspective on the synergistic possibilities of these capabilities and nanofabrication.

[1] K.Hoeflich et al., Appl. Phys. Rev. 10, 041311 (2023)

10:30am **MS-FrM-10 Efficient 3D Printing: Investigating Wall Count as an Alternative to High Infill Density in PLA, PET-G, and PA-CF**, ***Devyn Fidel,*** *M. Rabea,* California State Polytechnic University, Pomona

An important aspect of 3D printing is using the proper slicer settings to ensure that the part printed will have the desired properties, i.e., tensile strength and print quality. While convention often highlights maximizing infill density to enhance strength, this study explores methods to achieve optimal tensile strength without resorting to 100% infill, which can be wasteful and economically inefficient—specifically, increasing the wall (or perimeter) count. Regarding slicer settings, walls refer to the number of perimeters printed concentrically around the contour of a part. Adding more walls can offer greater strength than traditional infill structures due to the alignment of walls along the primary load-bearing axis using the same amount of material. This study compared the tensile strength of 3D-printed PLA, PET-G, and PA-CF specimens. One set of specimens had varying wall counts, and the other group had varying infill densities. The data showed that increasing wall count offers superior strength to traditional infill structures using less material.

10:45am **MS-FrM-11 Sustainable Microelectronics in the Age of Ai**, ***Emre Salman,*** Stony Brook University **INVITED**

Artificial Intelligence (AI) is increasingly pivotal in advancing the sustainability of microelectronics. It not only enhances energy efficiency through the discovery of innovative materials, devices, manufacturing technologies, but also optimizes the design automation of complex microelectronic systems. Beyond microelectronics, AI significantly contributes to environmental sustainability, notably in optimizing smart grids and advancing climate modeling to predict changing patterns more accurately. Despite these benefits, AI algorithms are executed on energy-intensive hardware platforms, predominantly housed in datacenters, which raises concerns about their environmental impact.

The energy footprint of AI hardware comprises two major elements: (1) the energy expended in the manufacturing of AI hardware, which predominantly uses advanced CMOS technologies facilitated by extreme ultraviolet (EUV) lithography, and (2) the operational energy consumption of datacenters, which includes both the computation and the cooling systems. This presentation will provide a comparative analysis of these critical components, emphasizing the significant energy demands of producing nanoscale CMOS-based integrated circuits and the substantial power used during computational tasks in datacenters.

To mitigate these challenges, the talk will explore a variety of innovative strategies and emerging technologies designed to reduce the energy footprint associated with both the manufacturing processes and the operational phases of AI hardware. The discussion will highlight recent advancements that promise greater efficiency and sustainability in the lifecycle of AI systems.

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