CHIPS Act Mini-Symposium
Room 122 - Session CPS-MoM

CHIPS Act Mini-Symposium

Moderators: Alain Diebold, University at Albany-SUNY, **Erica Douglas**, Sandia National Laboratories, **Timothy Gessert**, Gessert Consulting

8:15am **CPS-MoM-1 Midwest Semiconductor Collaborative Network for Work Force Training (MSN Force)**, *G. Tutuncuoglu,* ***Alireza Moazzeni,*** Wayne State University

The U.S. semiconductor industry's workforce is expected to grow by nearly 115,000 jobs by 2030, increasing from approximately 345,000 jobs today to about 460,000—representing a 33% rise. In response to this demand, the Midwest Semiconductor Collaborative Network for Workforce Training (MSN Force), funded by the National Science Foundation (NSF), aims to address the urgent need for highly skilled workers in the semiconductor sector, particularly within the Midwest. With a broader long-term vision of meeting national workforce development and R&D needs in semiconductor and microelectronics, MSN Force seeks to promote U.S. leadership in this critical industry.

Led by Wayne State University, MSN Force brings together a consortium of key academic institutions including Ohio State University, University of Michigan, Purdue University, Lorain Community College, and Youngstown State University. Our industrial and research partners, spanning organizations such as Synopsys, Intel, Mercedes Benz, NASA Glenn Research Center, SMART Microsystems, and the Semi Foundation, play a vital role in this initiative.

MSN Force focuses on co-developing training activities through close academia-industry partnerships, with an emphasis on experiential learning and robust industry engagement. The program integrates hands-on learning across all phases of semiconductor production, from device simulation and chip design to packaging, assembly, and testing. The ultimate goal is to create a comprehensive, state-of-the-art workforce training program that equips trainees with the skills needed to meet the evolving demands of the semiconductor industry.

8:30am **CPS-MoM-2 Opportunities and Challenges for Interdisciplinary Research and Education in Microelectronics**, ***Ashok Kumar,*** University of South Florida

As evident from the 2022 CHIPS and Science Act and the 2020 National AI Initiative Act, there is an acute need for talented and trained workforce in semiconductor manufacturing and Artificial Intelligence (AI)/Machine Learning (ML) areas. Recent NSF NRT (National Research Traineeship) grant has provided support to develop and implement a comprehensive and experiential learning-based education, research, training, and skills development program in semiconductor design, manufacturing, and packaging. This talk will provide interdisciplinary semiconductor concepts and emerging technologies that will be integrated in existing courses with novel experiential lab training in Class 1000 cleanroom environment.Students will be involved with industrial partners to define research problems using a convergence approach to design and develop application-driven semiconductor systems and devices. This program is innovatively designed such that the students on completion will gain essential competencies, namely, transdisciplinary knowledge, communication, teamwork, experimental & computational skills, informed decision making, entrepreneurship skills, project management, ethics, leadership, and safe and sustainable manufacturing. Students with entrepreneurial interest will have the opportunity to complete NSF I-Corps site training. In summary, this presentation will provide on-going development and implementation of a new interdisciplinary curriculum, featuring novel courses in fundamentals of materials, processing, metrology, device fabrication with specific applications to semi-conductor technology development.

8:45am **CPS-MoM-3 Strategic Roadmapping for Information and Communication Technologies**, ***Victor Zhirnov,*** Semiconductor Research Corporation*; V. Zhirnov,* SRC **INVITED**

Information and Communication Technologies (ICT) is the social-economic growth engine of the modern world. This electronic processing and transmission of information includes the explosion of sensing for real-world applications in many market segments, such as automotive, industrial manufacturing and automation, robotics, health, environmental, etc. The use of ICT continues to grow without bounds driven by the exponential creation of data that must be moved, stored, computed, and communicated. Ever-rising energy demands for information and communication technologies versus global energy production are creating new risks. Therefore, new paradigms need to be discovered in order to dramatically improve energy efficiency of ICT.

In the past, the role of strategic planning for semiconductor industry was met by the International Technology Roadmap for Semiconductors (ITRS), serving as a master plan that provided manufacturers, designers, and equipment suppliers with direction years in advance. By providing a common framework for coordination across semiconductor industry stakeholders, technology development efforts were efficient and aligned. However, the dissolution of the ITRS in 2015 left a void, leading to years of disjointed efforts. Recognizing the need for unified guidance, the industry rallied for the creation of new strategic plans, which yielded the 2030 Decadal Plan for Semiconductors (identifies the “What”) and the Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap (identifies the “How”) were developed. These comprehensive plans outline ambitious goals for the industry's future.

Inventing the next hardware/software ICT paradigm is a tall order. However, it is achievable if the right questions are asked and the right resources are put in place. These steps are outlined in the Decadal Plan and in the MAPT Roadmap, which emphasize the need for radical new solutions for future ICT, including sustainability and workforce development.

9:15am **CPS-MoM-5 Challenges and Opportunities in Characterization and Metrology for the Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap**, ***Markus Kuhn,*** Rigaku*; A. Diebold,* SUNY Polytechnic Institute, Albany **INVITED**

The recently released Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap represents the collective efforts of hundreds of individuals representing >100 organizations from government, academia, and industry. The MAPT Roadmap directly supports the Chips and Science Act, led by the U.S. Department of Commerce, in efforts to develop a robust domestic semiconductor ecosystem.

The metrology chapter describes the characterization and metrology requirements for all areas of the MAPT Roadmap including Materials and Devices through Advanced Packaging and Heterogeneous Integration and Systems.Metrology measurements enable all aspects of semiconductor materials and device research, development, and manufacturing, therefore making support for this area critical to meeting technology objectives.

This talk will highlight the importance of continued metrology development and assess the key challenges facing this segment for the next 10+ years. Some of the key challenges and initiatives are highlighted below.

1. Manufacturing-ready 3D metrology.
2. Lab to fab transition to introduce new capabilities into manufacturing.
3. Accelerating lab metrology output (wafer coverage, precision, throughput).
4. Enabling and incorporating DFM (design for metrology,) ML/AI, hybrid metrology concepts as part of a holistic process, test, and simulation ecosystem.

9:45am **CPS-MoM-7 CHIPs Act and Optoelectronics, Devices, and AI/ML**, ***Volker Sorger,*** University of Florida **INVITED**

What is the CHIPS ACt?The bipartisan CHIPS and Science Act signed into action in 2022 was a seminal action; for the first time since World War II (i.e. the Manhattan project) an economic stimulus package for a single industry was signed. The federal focus to re-shore manufacturing capabilities ($39B) along with R&D and workforce stimulus packages ($11B) is joined by matching funds from the States and the private sector (i.e. corporations, SMEs, venture capital), thus adding multiplication factors to the semiconductor ecosystem.

Why now? Chips having been invented in the U.S. some sixty years ago, have been off-shored since the 2000’s to far Asia, mainly due to economic factors. The resulting technological- and supply chain independence became all-too evident during the COVID years. With semiconductors (i.e. chips) being a critical part of modern businesses in virtually all economic sectors, securing and re-vitalizing manufacturing capabilities along with critical R&D projects are timely and, thankfully underway.

What is the Role of Photonics in Chips?Optics provides synergistic and performance extending capabilities in two major ways: a) data interconnects and b) special purpose computing. Optical Interconnects and

Advanced Packaging: Starting with the former, the bosonic nature and 1,000x wavefunction difference between photons and matter offers optics to provide low-loss long-distance data links. Unlike fibers, new to the CHIPS activities are that photonics is now considered inside board and even insider the package; the latter stems from the desire to blur-the-lines between what is in the package vs. what is on the board in advanced packaging. In addition to 2.5D interposer (e.g. active optical interposer) packaging strategies, 3D heterogenous integration (3DHI) solutions are anticipated to provide not just 100x interconnect performance gains (e.g. in units of [Gbps/mm/pJ/bit]), but also enable best-of-both world co-design and optimization 'options' (i.e. 'known-best-die'). In regard to Special Purpose Computing, photonic chips offers some interesting benefits but also challenges: the benefits resolve around the ability to i) executing mathematical functions in the optical domain at zero energy, ii) processing data at full bit resolution in their natural domain (no analog-to-digital conversion past the sensor), iii) allowing for high degrees of signal fan-out (e.g. for neuromorphic computing), and iv) enabling real-time computing in the 10's of picosecond range per device (minus RC delays from the optoelectronic components).

10:30am **CPS-MoM-10 Bridging Opportunities and Challenges: Examining a Community College's Role in Preparing Technicians for the Semiconductor Industry***, **Nancy Louwagie**,* Normandale Community College **INVITED**

Community colleges offer the potential to take on a crucial role in preparing the technician workforce for the semiconductor industry. This presentation aims to showcase a vacuum technology program offered at Normandale Community College (Bloomington, MN) as a case study, illustrating how such institutions can serve as hubs for workforce development. Furthermore, it delves into the obstacles faced by community colleges in establishing and sustaining high-tech programs of study.

Opportunities:

1. Affordability: Community colleges are recognized as the most cost-effective option in higher education, offering accessible pathways to technical education.
2. Accessibility: With campuses spread across states, community colleges ensure geographical inclusivity, providing equitable access to post-secondary education.
3. Localized Programming: Community colleges have the flexibility to tailor programs to meet the specific workforce demands of their regions.
4. Industry Collaboration: Increasingly, local employers are partnering with community colleges to provide internship and apprenticeship opportunities that enhance students' practical skills and employability prospects.

Challenges:

1. Financial Sustainability: Community colleges grapple with financial instability, particularly small programs, which are at constant risk of closure, threatening the continuity of any technician training program.
2. Faculty Recruitment: Technical programs require specialized faculty, but community colleges often struggle to attract and retain qualified instructors.
3. Equipment Procurement: Maintaining up-to-date equipment for hands-on learning is essential in technical education, yet community colleges face challenges acquiring and maintaining this equipment.
4. Pandemic Impact on Disadvantaged Students: COVID-19 exacerbated existing disparities, disproportionately affecting students from disadvantaged backgrounds. Academic setbacks pose challenges to program retention and completion rates.

Conclusion: Community colleges can fulfill a critical role in meeting the substantial technician development demands of the semiconductor industry. They are known for delivering affordable, accessible, and regionally tailored programs. However, sustaining and enhancing these initiatives requires addressing financial constraints, faculty shortages, equipment needs, and supporting students, particularly those facing pandemic-related setbacks. Collaborative efforts between educational institutions, industry partners, and policymakers are essential in navigating these challenges and maximizing the potential of community colleges in preparing the semiconductor workforce of tomorrow.

11:00am **CPS-MoM-12 CHIPS Act and the Future of the Semiconductor Industry Panel Discussion***, **Erica Douglas**,* Sandia National Lab

Leading experts will participate in CHIPs Act panel session chaired by Erica Douglas. The panel session will explore aspects of the new initiatives in the semiconductor industry funded by the CHIPs Act. Participants will include the invited speakers for the Chips Act Session.

CHIPS Act Mini-Symposium
Room Central Hall - Session CPS-ThP

CHIPS Act Mini-Symposium Poster Session

CPS-ThP-1 Expanding the AVS Science Educators Workshop to Historically Underserved Communities to Support Needs of the CHIPS in Science Act, ***Timothy Gessert***, Chair - AVS Education Committee

For ~30 years the AVS has trained groups of high-school teachers in vacuum technology through the Science Educators Workshop (SEW). This training also provides teachers with a small vacuum system designed for classroom demonstrations. The SEW training occurs at the annual International Symposium of the AVS, with travel and lodging paid for by a combination of funds from National AVS Education Committee and Regional AVS Chapters. It is estimated that between 500-1000 kits have been distributed to high-schools across the US during the past ~30 years. Although the SEW is viewed as an important AVS educational outreach activity to secondary-school educators, discussions with SEW teachers has suggested that the majority of teachers come from relatively well-funded school districts. Discussions with SEW Committee and AVS regional chapter members has further suggested, while many school districts strongly support continuing education for their teachers (such as the SEW), others are much less able to do this because of financial constraints. These realizations prompted the AVS to consider how future SEW-like activities might be designed to better align with the needs and resources of "Historically Underserved Communities" (HUCs). To pursue this goal, the AVS submitted a multi-year Venture Fund proposal to the American Institute of Physics, and this proposal was funded starting in 2021. Project goals include: (1) Understand the locations and needs HUCs better; (2) Determine how the AVS SEW might reach out to HUCs more effectively; and (3) Understand how the AVS SEW might modify its content and delivery methods to better align with HUC needs. Although these goals were designed in 2021 to improve the AVS SEW, it has recently been noticed that these goals reflect Workforce Development Guidance associated with Chips in Science Act (passed in 2022, with implementation starting in 2023). This presentation will describe ongoing progress in the AVS/AIP Project, focusing on lessons learned that may assist similar efforts in AVS Workforces Development activities related to the Chips in Science Act.

Author Index

Bold page numbers indicate presenter