Patterning improvement and oxidation mitigation of $Nb_xTi_{(1-x)}N$ metal lines processes for Superconducting Digital Logic Illustrations

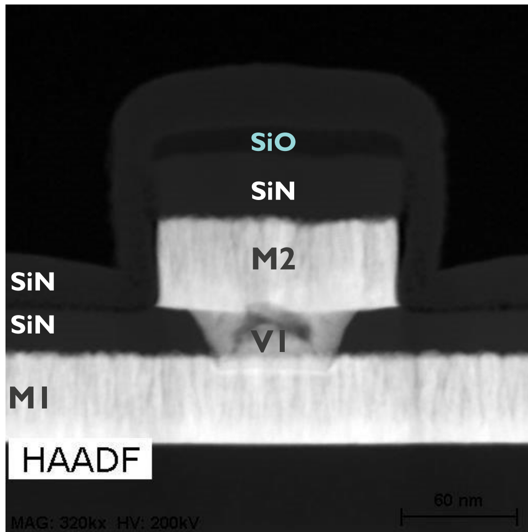

Figure 1: TEM image of a two-metal level BEOL device using $Nb_xTi_{(1-x)}N$ (NbTiN) for the metal lines (M1, M2) and Via (V1)

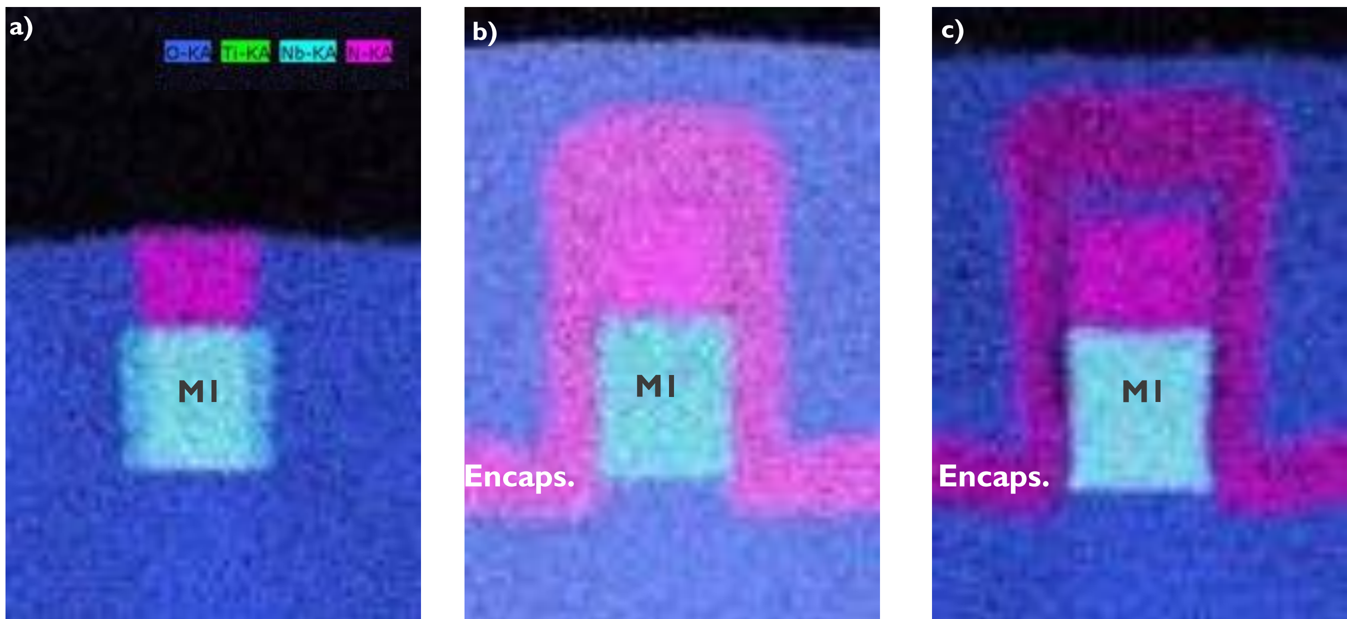

Figure 2: EDS analysis of $Nb_xTi_{(1-x)}N$ metal line (M1) a) without post-etching treatment, using aC as a hard mask (HM) to pattern NbTiN ; b) with wet oxide removal followed by an ex situ SiN encapsulation of M1, using aC as HM ; c) with post-etch in situ SiN encapsilation and using SiO_x as HM to pattern NbTiN