# AVS 70 abstract - Illustrations

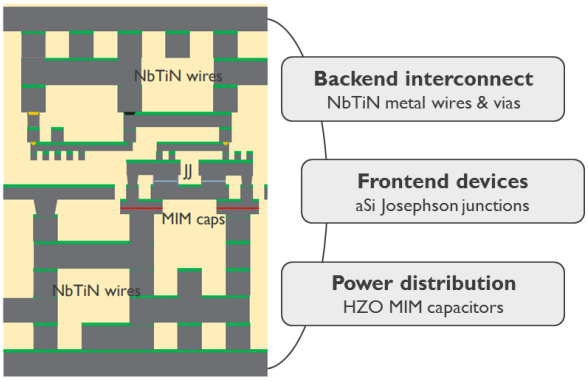


**Figure 1** : Main building-blocks scheme of SDL circuit

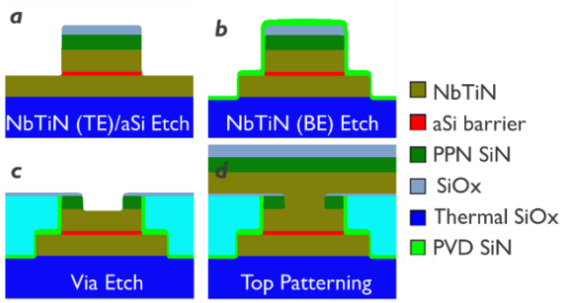


**Figure 2** : JJ device fabrication scheme; a) TE and αSi etch, b) BE etch, c) Via and d) Top patterning

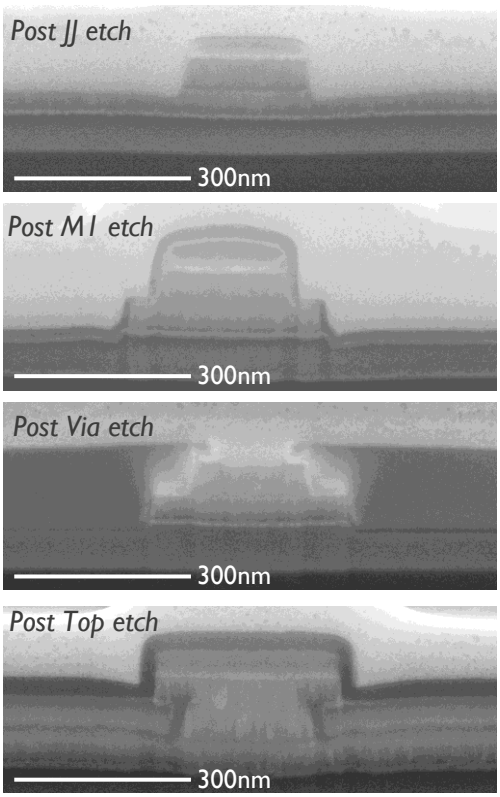


**Figure 3** : Step-by-step monitoring of JJ device fabrication

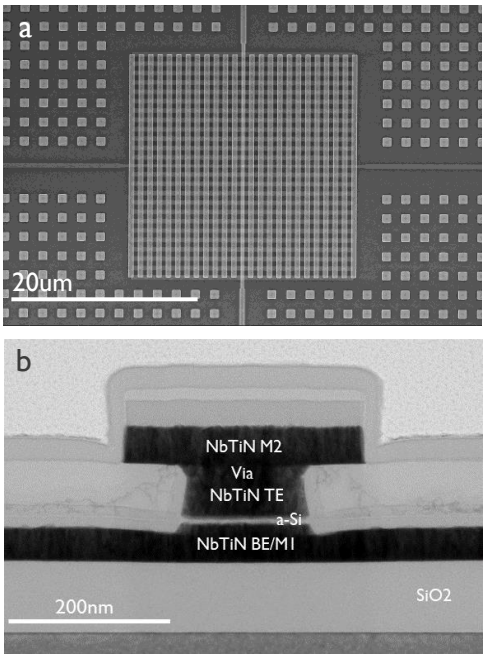


**Figure 4** : TD-SEM (a) and Cross section BF-TEM (b) of a representative 210nm device after compete device fabrication

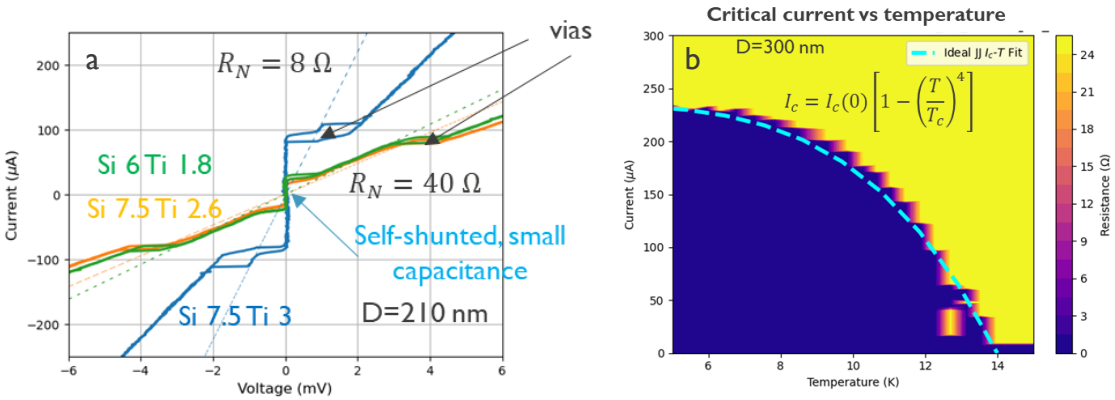


**Figure 5** : Representative IV curves of JJ device (210nm) at cryo T (a) and Representative IT plot of JJ device (300nm)