Quantum Science and Technology Mini-Symposium
Room 123 - Session QS2+PS-MoA

Advanced Fabrication and Plasma Techniques for Quantum Applications

Moderators: Angelique Raley, TEL Technology Center America, **Sebastian Engelmann**, IBM T.J. Watson Research Center, **David Pappas**, Rigetti Computing

4:00pm **QS2+PS-MoA-11 High-Rate (>50 nm/hour) Plasma-Enhanced ALD of Superconducting NbxTi1-xN with Substrate Biasing for Quantum Technologies***, **Silke Peeters**, L. Nelissen,* Eindhoven University of Technology, Netherlands*; D. Besprozvannyy,* Oxford Instruments Plasma Technology, UK*; N. Choudhary,* University of Glasgow, UK*; C. Lennon,* Oxford Instruments Plasma Technology, UK*; M. Verheijen,* Eindhoven University of Technology, Netherlands*; M. Powell, L. Bailey,* Oxford Instruments Plasma Technology, UK*; R. Hadfield,* University of Glasgow, UK*; E. Kessels,* Eindhoven University of Technology, Netherlands*; H. Knoops,* Oxford Instruments Plasma Technology, UK

The advancement of a wide range of quantum technologies hinges on improvements in materials and their interfaces. Plasma-enhanced atomic layer deposition (PEALD) enables the growth of high-quality superconducting thin films with atomic-scale control. Scalable integration of PEALD in the diverse field of superconducting quantum device fabrication requires the development of versatile, high-throughput processes.

We demonstrate PEALD of superconducting $Nb_xTi_{1-x}N$ films at a high rate of > 50 nm/hour on the Oxford Instruments PlasmaPro ASP system. The RF-driven remote capacitively coupled plasma (CCP) ALD system with small chamber volume allows for low-damage conditions and short cycle times. The CCP source is combined with RF substrate bias functionality allowing for ion-energy control. The depositions consist of NbN and TiN supercycles using the TBTDEN and TDMAT precursors and an $Ar/H_2/N_2$ plasma at a table temperature of 320 °C.

$Nb_xTi_{1-x}N$ films are prepared with film thicknesses ranging from 5 to 100 nm with < 5 % non-uniformity on a 150 mm diameter wafer. Four-point probe measurements yield low room-temperature resistivities increasing with Nb content from 160 µΩ cm (41 nm TiN) to 284 µΩ cm (25 nm NbN). The films are stoichiometric with a low ~2 at.% O impurity content. Accurate $Nb_xTi_{1-x}N$ composition control through supercycling is demonstrated from x=0 to x=1, with the C content increasing from 10 at.% to 19 at.% and the N content correspondingly decreasing from 40 at.% to 26 at.%. EDX mapping confirms homogeneous mixing of Ti and Nb and XRD reveals all prepared films are fcc polycrystalline. The crystallinity and conductivity of the films can be tuned by RF substrate biasing. TEM imaging of the most conductive 50 nm $Nb_{0.5}Ti_{0.5}N$ film prepared with 90 V bias reveals a disordered polycrystalline film in agreement with XRD, which shows peak broadening beyond 50 V bias.

$Nb_{0.5}Ti_{0.5}N$ films of 5 nm to 100 nm thickness display superconducting transitions at critical temperatures of 3.5 K to 10 K. A high sheet kinetic inductance of 470 pH/sq is found for the 5 nm film prepared with 90 V bias. Superconductivity is also confirmed for all explored compositions and substrate bias voltages. As a result, the film properties can be tailored whilst maintaining the high quality required for quantum applications. The novel ALD configuration negates the need for long plasma exposures to achieve this quality. This tunability and high rate of the $Nb_xTi_{1-x}N$ deposition process puts forward PEALD as a promising technique to tackle material challenges in a wide range of quantum technologies.

4:15pm **QS2+PS-MoA-12 Plasma etch study of NbTiN/αSi/NbTiN Josephson Junctions for Superconducting Digital Loic***, **Yann Canvel**, S. Kundu, V. renaud, A. Pokhrel, D. Lozano, D. Vangoidsenhoven, B. Kennens, A. Walke,* IMEC Belgium*; A. Herr,* IMEC

In the development of next-generation logic devices, an attractive complement to CMOS technology would be to leverage the superconducting technology which operate at a low temperature. Superconducting Digital Logic (SDL) devices are attractive as they are inherently faster and have much less power dissipation than their CMOS counterpart. Although SDL devices have existed for decades now, there have been fundamental challenges to scale down its main components and related interconnects. To provide groundwork for exploring SDL device integration, and a possible hybrid integration of SDL/CMOS circuits, one of the key patterning challenges is the Josephson Junction (JJ) device fabrication. JJ devices are the active devices of SDL technology that can potentially provide computational density, energy efficiency and interconnect bandwidth beyond conventional electronics.

In this communication, an in-depth plasma etch investigation is reported to demonstrate the patterning of high-density junctions with diameters between 210-500nm and CD control of <2% across the 300mm wafer. Using the Reactive Ion etching (RIE) technique, the study has firstly consisted of developing a non-standard NbTiN etch process which enables to pattern the JJ pillars through the Top Electrode (TE) and the αSi barrier, down to the Bottom Electrode (BE) with a precise etch landing control. Subsequent etch processes have then required successive engineering optimization to build up the final device. Some of the main challenges to tackle were the etch residues mitigation, the reduction of oxidized NbTiN interfaces and the final electrical contact with the Top metal. The successful fabrication of high density NbTiN/αSi/NbTiN junctions has offered the first demonstration of a Josephson Junction compatible with CMOS BEOL. Some electrical measurements at room and cryogenic temperatures will complete the investigation by showing high critical current, high speed and device stability up to 420°C.

Pokhrel, A *et al.,* First Demonstration of High Density NbTiN/αSi/NbTiN Josephson Junctions. *IEEE Symposium on VLSI Technology & Circuits (VLSI), (2024).*

Pokhrel, A. *et al.* Towards Enabling Two Metal Level Semi-Damascene Interconnects for Superconducting Digital Logic: Fabrication, Characterization and Electrical Measurements of Superconducting $Nb_xTi_{(1-x)}N$. *IEEE International Interconnect Technology Conference (IITC)*, (2023).

Holmes, D. S. *et al.* Energy-Efficient Superconducting Computing - Power Budgets and Requirements. *IEEE Transactions on Applied Superconductivity* **23**, 1701610–1701610 (2013).

Herr, Q. P. *et al.* Ultra-low-power superconductor logic. *Journal of Applied Physics* **109**, 103903 (2011).

4:30pm **QS2+PS-MoA-13 Patterning Improvements and Oxidation Mitigation of $Nb_xTi_{(1-x)}N$ Metal Lines Processes for Superconducting Digital Logic***, **Vincent Renaud**, Y. Canvel, A. Pokhrel, S. Iraci, M. Kim, B. Huet, J. Soulie, S. Sarkar, Q. Herr, A. Herr, Z. Tokei,* IMEC, Belgium

One promising alternative to standard CMOS technology is Superconducting Digital Logic (SDL) which enables computing at cryogenic temperature and, thus, performs faster at a reduced cost and power. Recently, it was demonstrated that a two-metal level BEOL unit process using $Nb_xTi_{(1-x)}N$ for the metal lines with a critical dimension of 50nm could be achieved on 300mm wafers. Cryogenic temperature electrical measurement showed that the lines and via of the device have a critical temperature of 12-13.4 K and a critical current density of 80-113 mA/µm^2. It was also highlighted that one of the crucial challenge in the making of this technology was the oxidation of the $Nb_xTi_{(1-x)}N$ metal lines during the direct metal etch process of the material itself and/or during the conception of the full device. This oxidation negatively impacts the electrical performance of the wire and could become a serious showstopper for the scalability of the device.

The goal of this study is to discuss different approaches for constructing and patterning the $Nb_xTi_{(1-x)}N$ metal lines while mitigating the oxidation of the device during the process. Different Hard-Mask (HM) materials have been investigated, as well as alternative HM removal processes. Finally, an in-situ encapsulation of the $Nb_xTi_{(1-x)}N$ metal lines post-etch process has been experimented to mitigate the oxidation the device when exposed to the air or during the sub-sequent dielectric gap-fill. These experiments were coupled with electrical measurements at room and cryogenic temperature with the aim of validating the best fabrication process for the $Nb_xTi_{(1-x)}N$ metal lines for SDL devices.

Pokhrel, A. *et al.* Towards Enabling Two Metal Level Semi-Damascene Interconnects for Superconducting Digital Logic: Fabrication, Characterization and Electrical Measurements of Superconducting $Nb_xTi_{(1-x)}N$. *IEEE International Interconnect Technology Conference (IITC)*, (2023).

Holmes, D. S. *et al.* Energy-Efficient Superconducting Computing - Power Budgets and Requirements. *IEEE Transactions on Applied Superconductivity* **23**, 1701610–1701610 (2013).

Herr, Q. P. *et al.* Ultra-low-power superconductor logic. *Journal of Applied Physics* **109**, 103903 (2011).

4:45pm **QS2+PS-MoA-14 Patterning of TiN and TaN for advanced superconducting BEOL***, **Thibaut Chêne**,* CEA-LETI, France*; R. Segaud, F. Nemouchi, S. Minoret,* CEA-Leti, France*; F. Gustavo,* CEA INP Grenoble, IRIG, France*; J. Garrione, T. Chevolleau,* CEA-Leti, France

The development of new quantum technologies based on superconducting Qubits or spin Qubits becomes a major subject of interest for applications in communication and data computing. Such technology operating at low temperature requires a superconducting rooting development.

The superconducting materials have been selected based on their superconducting properties and their integration capabilities in an industrial process flow. The integration is based on a top down approach by patterning successively both metals with a selective etch process to define lines and vias.

To develop the patterning process, a 40 nm thick film of TiN or TaN is deposited by PVD on a SiO_2 layer over 300 mm silicon wafers. Then the lithography is performed on a 193nm stepper to achieve 150 nm line and via critical dimension (CD). Etching developments are carried out on a 300 mm industrial ICP chamber using Cl_2 chemistry with or without HBr or CH_4 addition. A parametric study of Cl_2 based chemistries is performed to achieve a straight profile with low CDbias and also to determine the selectivity of TaN over TiN. Optical Emission Spectroscopy (OES) and quasi in-situ Xray Photo-electon Spectroscopy (XPS) are conducted to better understand the etching mechanisms.

Regarding the TiN, straight profiles and good CD control are achieved with Cl_2/HBr chemistries but micromasking is observed. The micromasking phenomenon will be further discussed in terms of plasma/surface interaction based on the quasi in-situ XPS analyses. The addition of CH_4 instead of HBr prevents the micromasking while keeping a rather straight profile with an etch rate of 70 nm/min. For the TaN, whatever the etching chemistries, lower etch rates are observed in comparison with TiN. This trend is attributed to a higher Ta-N binding energy and lower etch by-product volatility. The Cl_2/HBr and Cl_2/Ar plasma chemistries lead both to CD loss and tapered profile mainly due to a lack of selectivity with the PR. Oppositely, the Cl_2/CH_4 chemistry allows achieving straight TaN profile by adjusting the amount of CH_4. The patterning of 80 nm vias for both TiN and TaN are obtained by combining resist trimming and the etching processes previously optimized for the narrow lines. After this patterning process optimization, the T_c of 150 nm CD structures is measured using a specific test vehicle for both TiN and TaN thin films. We will then leverage the TiN:TaN etching selectivity of 4.6 achieved by tuning the Cl_2/CH_4 amount to integrate TiN vias on TaN lines.

5:00pm **QS2+PS-MoA-15 Optimization of Superconducting Transition Metal Nitride Films Deposited by Reactive High-Power Impulse Magnetron Sputtering***, **Hudson Horne**, C. Hugo, B. Reid, D. Santavicca,* University of North Florida

Ultra-thin films of transition metal nitrides are used to create superconducting devices such as superconducting nanowire single-photon detectors, kinetic inductance detectors, and parametric amplifiers. Nanowires made from such materials also have applications in quantum computing, for example as high-impedance, low-dissipation shunts to suppress charge noise in superconducting qubits. In this work, we explore the use of high-power impulse magnetron sputtering (HiPIMS) to optimize the superconducting properties of transition metal nitride thin films for such device applications.

Initial work has focused on niobium nitride deposited using a reactive process in which a niobium target is sputtered in the presence of nitrogen gas. We compare films deposited on silicon substrates via HiPIMS and conventional DC sputtering, and we find that HiPIMS can produce films of the same thickness with a higher critical temperature and a lower normal-state resistivity. Film composition and structure are characterized with scanning electron microscopy, wavelength-dispersive x-ray spectroscopy, and x-ray diffraction, and these results are correlated with the electrical properties of both unpatterned films and nanowires. These characterizations suggest that the improved superconducting properties of the HiPIMS films is the result of optimizing the stoichiometry in the desired δ crystal phase. We show that further improvement in the critical temperature is possible through the use of an aluminum nitride buffer layer and through substrate heating.

We have begun extending these studies to other materials such as titanium nitride and hafnium nitride. This work seeks to systematically explore the HiPIMS process for optimizing transition metal nitride films with an emphasis on ultra-thin films for quantum device applications.

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