Plasma Science and Technology
Room 124 - Session PS2-WeA

Plasma Processes for Emerging Device Technologies

Moderator: Phillipe Bezard, IMEC Belgium

4:15pm **PS2-WeA-9 Low Damaged GaN Surface Through Passivating Plasma Etching and Post-Etch Treatments for Improved GaN-MOS Capacitor Performance**, ***David Cascales,*** CEA-LETI & LTM, France; *P. Pimenta-Barros, E. Martinez,* CEA-LETI, France; *B. Salem,* LTM - MINATEC - CEA/LETI, France

The power electronics industry is facing new challenges to meet the increasing needs of electrical power in modern devices[1]. These needs require an efficiency rise of power converters, also accompanied by higher operating voltages, currents and frequencies. Wide bandgap materials such as GaN are then investigated and preferred to Si-IGBT converters due to silicon limits being reached[2]. Lateral and vertical GaN-based power devices have emerged such as the vertical MOSFET or the lateral MOS-channel High Electron Mobility Transistor (MOSc-HEMT). With both technologies, normally OFF properties are needed and can be achieved with a gate recess, while a MOS gate controls the channel operation.

Plasma processing is crucial for channel and gate performance[3]. For instance, the recess shape can directly affect channel conducting properties and gate leakage, while the damaged GaN layer can influence the gate's behavior by deteriorating the flat band voltage. Indeed, flat band voltage is driven by charge generation that is caused by lattice amorphization, nitrogen depletion, element implantation or etching by-products deposition[4].

This study aims to investigate negative charge generation at the GaN/dielectric interface in order to shift threshold voltages towards greater values. Plasma etchings and post etch treatments (PET) were performed in an ICP chamber, together with pre-deposition treatments in the ALD chamber prior to dielectric deposition to limit nitrogen depletion and lattice amorphization.

First, thanks to X-ray Photoelectron Spectroscopy measurements, we will discuss the chemical modifications induced by silicon introduction ($SiCl_4$) in a Cl_2 plasma etching chemistry. A Si-based layer protecting GaN from ion bombardment is present at the Al_2O_3/GaN interface. The Si-layer and GaN evolution through the MOS capacitor fabrication steps will then be analyzed, including the O_2 PET, and the Al_2O_3 ALD preceded by an HCl gallium oxide removal. $SiCl_4$ addition shows a significant flat band voltage improvement with C-V measurements. As well, HCl replacement by a dry *in situ* N_2/H_2 pre-deposition treatment for high $SiCl_4$ etching ratios will also be examined.

Finally, we will explore the impact of PET chemistry variations after $SiCl_4/Cl_2$ etching with addition of N_2 to the O_2 chemistry, giving a better understanding of the plasma interactions with GaN, the SiN holder and chamber walls. The goal is to restore the N/Ga ratio with nitrogen supply.

[1]International Energy Agency (IEA), World Energy Outlook (2022)
[2]E. A. Jones et al., *IEEE WiPDA* (2014)
[3]S. Ruel *et al.*, *J. Vac. Sci. Technol. A*, 39(2), p. 022601
[4]P. Fernandes Paes Pinto Rocha, *Energies*, 16(7), p. 2978

4:30pm **PS2-WeA-10 Anisotropic and Sub-Micrometric InGaP Plasma Etching for High Efficiency Photovoltaics**, ***Alison Clarke***, *M. de Lafontaine,* University of Ottawa, Canada; *R. King, C. Honsberg,* Arizona State University; *K. Hinzer,* University of Ottawa, Canada

Nanoscale III-V semiconductor etching enhances light trapping, enabling low cost and efficient photovoltaic devices [1]. Mitigating sidewall erosion and chlorine-based defects is crucial for increased device performance. However, anisotropic III-V patterning with sub-micrometric definition has many challenges, such as sidewall erosion and surface damage [2]. Room-temperature InGaP plasma etching is challenging due to non-volatile $InCl_x$ subproducts. Chlorine-based plasmas lead to defects which can be passivated by introducing hydrogen-based plasma chemistries [3].

InGaP nanotextures with vertical sidewalls were patterned using electron-beam lithography and inductively coupled plasma etching. Circular nanotextures with 850 nm diameter and 150 nm minimum spacing were patterned in a hexagonal array. The etch was performed at room temperature to limit sidewall erosion [3], using the resist as a mask. To assess the impact of chlorine and hydrogen, four plasma chemistries were investigated: Cl_2/Ar, Cl_2/H_2, Cl_2/Ar/H_2, and Ar/H_2. The etched InGaP was investigated with atomic force microscopy. The Cl_2/H_2 plasma produced the fastest average etch rate (150 nm/min), with aspect ratio of 0.66. The Ar/H_2 plasma had the slowest average etch rate (75nm/min) due to the absence of Cl-based chemical etching. All etch rates were low due to the high (~25%) In content in the InGaP which creates poor volatility byproducts. Hydrogen improved the etching process, suppressing chlorine-based defects and decreasing the line edge roughness by up to 48% compared to the plasma without hydrogen.

These results show that hydrogen-based plasma chemistries improve pattern transfer for photovoltaics applications, where precise control of critical dimensions is required to improve conversion efficiencies. Ongoing work on top view and cross-sectional scanning electron microscopy will also be presented along with device performance measurements to confirm light-trapping properties. Complimentary characterizations such as energy-dispersive X-ray spectroscopy will be performed to benchmark the passivation properties of hydrogen plasmas.

[1] N.P. Irvin et al., "Monochromatic Light Trapping in Photonic Power Converters," *49th IEEE Photovoltaics Specialists Conference,* 0143 (2022).

[2] M. Bizouerne et al., "Low damage patterning of In0.53Ga0.47As film for its integration as n-channel in a fin metal oxide semiconductor field effect transistor architecture," *J. Vac. Sci. Technol.*, 36(6):061305 (2018).

[3] M. de Lafontaine et al., "Anisotropic and low damage III-V/Ge heterostructure etching for multijunction solar cell fabrication with passivated sidewalls." *Micro Nano Eng.*, 11:100083 (2021).

4:45pm **PS2-WeA-11 On the Plasma Etching Mechanisms of Patterned Aluminum Nitride Nanowires with High Aspect Ratio**, ***Saron Sales de Mello***, *L. Jaloustre,* University Grenoble Alpes, CNRS, LTM, France; *S. Labau, C. Petit-Etienne,* University Grenoble Alpes, CNRS,LTM, France; *G. Jacopin,* University Grenoble Alpes, CNRS, Institut Néel, France; *E. Pargon,* University Grenoble Alpes, CNRS, LTM, France

III-nitride (III-N) semiconductor light-emitting diodes (LEDs) are a particularly promising alternative to mercury vapor lamps as ultra violet (UV) sources [1]. However, the external quantum efficiency (EQE) of current planar Al_xGa_yN well-based UV LEDs is extremely low (<1% for wavelengths below 250 nm)[2]. Three-dimensional (3D) core−shell architecture offers some promising solutions to increase UV LED efficiency up to 50%.This approach consists in radially growing emissive quantum wells on predefined aluminum nitride (AlN) nanowires (Fig.1) [3]. The top-down combining lithography and plasma etching transfer is the only viable approach to fabricate the well-organized arrays of high Aspect Ratio (AR) AlN nanowires required.

This study aims to develop a chlorine (Cl_2) plasma etching process in a Inductively Coupled Plasma (ICP) reactor dedicated to high AR AlN nanowires (AR>10, i.e. sub-500nm diameters, 4µm-high) fabrication, based on a fundamental understanding of the etching mechanisms involved. The samples are AlN (4µm) grown on sapphire substrate with a silicon oxide (SiO_2) 1.4µm thick hard mask on top. Electron beam lithography is used to design dots with several diameters, densities and shape. We investigate the impact of the plasma parameters (source, bias and pressure) on the AlN etch rates, AlN/SiO_2 etch selectivity, pattern profiles and sidewalls roughness. We observe that the carrier wafer (CW) chemical nature (Si or Si_3N_4) affects the nanowire profile. Under the same plasma conditions, the use of Si_3N_4 CW always leads to passivation layer formation on the AlN sidewalls, which creates more tapered AlN pillars than using Si CW (Fig. 2). In both cases SiClx etch by products coming from the CW are present in the plasma and are likely to redeposit on AlN sidewalls [4]. However, with Si_3N_4 CW, the presence of N helps to fix the SiClx and to form a SiNCl passivation layer.

Ion flux, ion angular distribution and ion energy measurements show that, the plasma conditions that favor high ion flux over radical flux (higher source power, lower pressure, higher bias) enhance the AlN etching, suggesting an ion-enhanced chemical etching mechanism. In addition, conditions for which the physical component of the plasma dominates lead to tapered profiles, while anisotropic ones can be obtained when the chemical component dominates. Fig. 3 shows the source power impact on the profiles. Charging and ion angular distribution effects also affect the pattern profiles. Finally, we also observe a crystal orientation preferential etching phenomenon. Cl_2 plasma etching tends to reveal nonpolar a-planes, suggesting that they are the most stable in this process.

5:00pm **PS2-WeA-12 Room Temperature ICP Plasma Passivation for SiC MOS Capacitor*, Rodrigo Cesar,*** Center for Electronic Components and Nanotechnology - CCSNano, Brazil

Studies on silicon carbide (SiC) began in the late 1980s. Initially used as an abrasive material in cutting tools, it has become a highly promising material in the microelectronics industry due to its properties such as high thermal conductivity, high breakdown voltage, large band gap, high electron saturation velocity, and high thermal conductivity. Therefore, it is ideal for developing devices that will used in extreme power and temperature conditions.

A crucial point in the process of manufacturing devices with SiC substrate is surface passivation. This process completes the open bonds of carbon ions, reducing the surface defects and charge density, resulting in devices with better performances. There are several passivation methods such as oxidation, nitridation, doping with phosphorus ions, among others. However, all these processes occur at high temperatures, with the most commonly used being treatment in a furnace at 1500°C. In this work, we propose a passivation process where the great advantage is to carry out the process at room temperature. For this, we employ an inductively coupled plasma – ICP, and different tests, using plasmas with N2 and N2+O2 gases in an ICP LAM equipment.

In order to evaluate these passivation processes, we manufacture MOS capacitors using HfO2 as the gate dielectric and Si wafers previously passivated, which were electrically characterized using C×V curves. Here we determined the best time and gas combination that results in the best passivation and consequently the best device performance. Table 1 presents a summary of the tests carried out and table 2 show the parameters used during the tests.

In Fig. 1A we can see a clear difference between the C×V curve of the sample with only N2 plasma and the others. In this way, this curve was removed, as shown in Fig. 1B, where we can observe that the curve improvements occurred post-oxidation annealing (POA), with the best treatment being N2+O2+POA.

With the best passivation determined, two SiC capacitors were manufactured, one with passivation and the other without. Fig. 2 shows the C×V curves of these capacitors. It can be seen that there was a significant difference between the curves. The one without passivation has a VFB of 9V, twice the size of the curve with passivation. The curve with passivation demonstrates the efficiency of the passivation process, presenting a well-defined C×V curve with a smaller range than that without passivation, in addition to the fact that the VFB value is 4V.

This indicates that room temperature passivation by ICP plasma is effective.

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