## Thin Films
## Room 115 - Session TF2+EM-ThM

### Thin Films for Microelectronics I: BEOL

**Moderators: Sarah Atanasov**, Intel, **Matthias Young**, University of Missouri

11:00am **TF2+EM-ThM-13 Inherently Selective Thermal Atomic Layer Deposition of Copper Metal Thin Films**, ***Charles Winter***, Wayne State University **INVITED**

The continued miniaturization of microelectronics devices has created the need for new high-performance materials and appropriate nanoscale deposition processes. Atomic layer deposition (ALD) is a growth technique that affords Angstrom level control of film thicknesses and can give perfect conformal coverage in high aspect ratio nanoscale features. Copper (Cu) is a central interconnect metal and its growth by ALD remains a topic of significant interest. Many Cu ALD processes have been reported, but most are limited to lower temperatures (<200 °C) because of limited thermal stability of the Cu precursors. Herein, we will describe a new thermal Cu ALD process that employs bis(2,2,6,6-tetramethyl-3,5-heptanedionate)copper(II) ($Cu(thd)_2$) and nitrogen compounds as precursors. Cu metal film growth trials were conducted between 175 and 300 °C using $Cu(thd)_2$ and hydrazine on a variety of substrates, including Ru, Cu, TiN, $SiO_2$, Si with native oxide, and Si-H. Self-limited growth of Cu films on Ru substrates was demonstrated at 225 °C for both $Cu(thd)_2$ and hydrazine, with a growth rate of about 0.25 Å/cycle. An ALD window was observed for this process between about 225 and 275 °C. The characterization of the Cu films will be overviewed, including compositions, resistivities, and surface morphologies. Inherently selective growth of Cu metal films was observed on metal substrates such as Ru, Cu, and TiN. No growth occurred on insulating substrates such as Si-H and $SiO_2$. Inherently selective growth of Cu films by ALD on metal substrates offers many new opportunities for metallization.

11:30am **TF2+EM-ThM-15 Effect of Hydrogen Annealing on Grain Growth of Tungsten Films**, ***Seunghyun Park***, School of Advanced Materials Science & Engineering, Sungkyunkwan University, Republic of Korea*; S. Kim,* Department of Semiconductor and Display Engineering, Sungkyunkwan University, Republic of Korea*; C. Park, H. Kim,* School of Advanced Materials Science & Engineering, Sungkyunkwan University, Republic of Korea

Tungsten (W) has been widely used for first level metallization in memory and logic devices due to its low electrical resistivity and high thermal stability. In addition, it can be easily deposited as an ultrathin film with high step coverage through chemical vapor deposition (CVD) or atomic layer deposition, rendering it suitable for complex device structures. However, the dimensional down-scaling of metal lines to less than 10−20 nm is accompanied by a simultaneous decrease in grain size, which results in an inevitable increase in the resistance due to enhanced surface and grain boundary scattering [1]. Therefore, one possible approach to maintain low resistivity of the ultrathin W film at small dimensions could be the introduction of additional thermal annealing that effectively increases the grain size while using a low temperature below 400 °C.

A couple of researchers observed abnormal grain growth of nickel and vanadium by introducing $H_2$ during the annealing process at high temperatures above 600 °C [2, 3]. Based on these findings, this presentation aims to explore the annealing of ultrathin W films in an $H_2$ environment at various temperatures (300−500 °C). To evaluate the effectiveness of H2 in increasing grain size, $N_2$ and high-pressure $H_2$ annealing were also introduced. The W film of 20 nm thickness was deposited using CVD on a $SiO_2$/Si substrate coated with a TiN adhesion layer. Grazing incidence X-ray diffraction measurements revealed that $H_2$ annealing at 1 bar resulted in an increased crystallite size, indicative of grain size, compared to $N_2$ annealing under all temperature conditions, which was accompanied by a decrease in resistivity. In addition, the increase in the $H_2$ pressure to 5 bar increased crystallite size further and reduced electrical resistivity accordingly.

[1] D. Gall, J. Appl. Phys. 127, 050901 (2020).

[2] T. Wagner et al., Int. J. Mater. Res. 93, 401−405 (2002).

[3] M. L. Martin et al., Acta Mater. 155, 262−267 (2018)

11:45am **TF2+EM-ThM-16 Textured Growth of Zinc Sulfide on Back-End-of-the-Line (BEOL) Compatible Substrates**, ***Claire Wu***, University of Southern California*; M. Surendran,* Lawrence Berkeley National Laboratory*; P. Tzeng, C. Wu, X. Bao,* TSMC, Taiwan*; J. Ravichandran,* University of Southern California

Scaling of transistors has enabled continuous improvement in the performance of logic devices, especially with recent advances in materials engineering for transistors. However, there is a need to surpass the horizontal limitations in chip manufacturing and incorporate the vertical or third dimension. To enable monolithic three-dimensional (M3D) integration of high-performance logic, one needs to solve the fundamental challenge of low temperature (<400 °C) synthesis of high mobility n-type and p-type semiconductor thin films that can be utilized for fabrication of back-end-of-line (BEOL) compatible transistors.1 Transition metal oxides are promising n-type materials; however there is a lack of p-type materials that can meet the stringent synthesis conditions of BEOL manufacturing. Zinc sulfide (ZnS), a transparent wide band-gap semiconductor, has shown room temperature p-type conductivity when doped with copper and crystallizes below 400oC when grown by pulsed laser deposition (PLD).2, 3 Here, we report growth of crystalline thin films of ZnS by PLD on a variety of amorphous and polycrystalline surfaces including silicon nitride, (SixNy) thermal silicon dioxide, (SiO2), hafnium dioxide, (HfO2) and titanium nitride (TiN). High-resolution thin film X-ray diffraction shows texturing of ZnS on all three substrates. Crystalline quality was investigated using rocking curve measurements. Surface and interface quality was measured using X-ray reflectivity and atomic force microscopy measurements. Further work in characterizing the film quality through electrical measurements such as conductivity and capacitance shall be discussed. This work showcases the capability of thin film growth of a wide band-gap semiconductor in BEOL compatible conditions with technological applications in transistor manufacturing.

References:

1. IEEE Micro. 2019, 39, 6, 8-15.

2. Adv. Electron. Mater. 2016, 2, 1500396

3. Adv. Mater.2024, 36, 2312620

12:00pm **TF2+EM-ThM-17 Steep-Slope IGZO Transistor with an Ag/$Hf_{1-x}Zr_xO_2$ Atomic Threshold Switch**, ***Junmo Park***, *D. Eom, H. Kim, Y. Kim, H. Kim,* Sungkyunkwan University, Republic of Korea

Atomic threshold switch (ATS) exhibits abrupt switching characteristics due to the formation of electrochemical metallization filaments by the diffusion of Ag or Cu atoms towardsthe dielectric [1].Recently, it has been consideredfor integration with a field-effect transistor (FET) to build a steep-slope FET that overcomes the conventional subthreshold swing (SS) limit of 60 mV/dec [2]. Up to now, various FETs implemented with Si, transition-metal dichalcogenide, and oxide channels have been actively adopted for integration with ATS devices [3]. Particularly, the steep-slope FET built with an indium gallium zinc oxide (IGZO) transistor isattracting great attention because its fabrication temperature is low enough to meet thethermal requirements of a back-end-of line (BEOL) process [4]. However, it was demonstrated not through monolithic integration but through electrical wiring after fabrication of individual devices [5].

In this presentation, we suggest a novel BEOL-compatible steep-slope FET where an IGZO transistor is monolithically integrated with an Ag/$Hf_{1-x}Zr_xO_2$ (HZO) ATS at less than 400 °C. The IGZO and HZO films were deposited using sputtering at room temperature and atomic layer deposition at 200 °C, respectively.The Ag/HZO ATS is connected to the drain electrode of the IGZO FET in series. The SS of IGZO transistors was controlled by varying the composition of the HZO film, resulting achievement of SS muchless than 60mV/dec.Furthermore, we found that the HZO film with a Zr content (x) of ~25% led to a lower threshold voltage compared to the same thickness $HfO_2$ single-layerand did not require a high voltage electroforming process (initialization). The detailed electrical characterization results of individual ATS, FET, and integrated ATS-FET devices will be discussed along with the physical and chemical characterization results of the HZO and IGZO films.

This work was supported by the GRRC Program of Gyeonggi Province (GRRC Sungkyunkwan 2023-B01)

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[3] Elahi et al., Mater. Today Phys. **30**, 100943 (2023).

[4] A. Choi et al., Chem. Mater. **36**, 2194 (2024)

[5] Cheng et al., Appl. Phys. Express **12**, 091002 (2019)

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