Electronic Materials and Photonics
Room Central Exhibit Hall - Session EM-ThP

Electronic Materials and Photonics Poster Session

EM-ThP-1 Optimizing Amorphous Indium Gallium Zinc Oxide Thin Film for Application in Photoactive Layers, ***Anvar Tukhtaev***, *J. Lee, J. Berdied, S. Kim,* Chungbuk National University, Republic of Korea

Amorphous metal oxide semiconductors are popular research targets due to their high performance and versatility, and are employed in a wide array of novel areas, including neuromorphic circuits. However due to the wide band gap of most metal oxides, their use in optoelectronics is very limited. Multiple methods for the fabrication of photodetectors with metal oxides have been considered in the literature, such as bilayer heterojunctions with photoactive materials and intentional defect formation to increase tail state density and reduce the band gap. Here, we demonstrate two approaches to improve the photoresponsive characteristics of amorphous indium gallium zinc oxide (a-IGZO)-based field-effect transistors. First, we prepare a bilayer of a thermally annealed a-IGZO and a polycrystalline PTCDI-C13 thin film, to combine the high mobility charge transfer of the metal oxide with the high photoresponse of the PTCDI-C13. The annealing temperature of the a-IGZO is optimized to achieve enhanced charge transport between the layers. Then, a gradient annealed a-IGZO thin film is prepared, in which a bottom layer of high temperature-annealed oxide film acts as the charge transport layer, which is complemented by a low temperature-annealed top layer. The higher disorder in the top layer increases the absorption of the film. The annealing temperatures are optimized to achieve highest mobility in the bottom layer and best photoresponse characteristics in the top layer. These methods demonstrate that metal oxides can be utilized in next-generation neuromorphic photodetection circuits such as on-hardware image recognition artificial intelligence applications.

Acknowledgements
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EM-ThP-2 Improvement of Al Undercut Defect in sub 20 Nm DRAM, ***DONG-SIK PARK***, *b. Choi,* Sungkyunkwan University (SKKU), Republic of Korea

In the era of the Fourth Industrial Revolution, the utilization of high-performance and high-speed DRAM is increasingly expanding. In response to this trend, the integration density of DRAM is also improving. Since transitioning to the 10 nm design rule, scaling is continuously demanded not only for the DRAM cell size but also for the wiring. The wiring, responsible for supplying electrical signals and power to the DRAM, consists of 4 to 5 layers, with the final wiring utilizing Al lines. Low resistance is necessary to accommodate the delivery of high power for the Al layers.

The composition of Al wiring is as follows: Ti is applied as a barrier metal to connect with the Via tungsten, followed by the formation of Al wiring with a thickness of over 500 nm using the PVD method. On top of this, TiN is applied as an anti-reflecting layer. The Al wiring is patterned using lithography and dry etching techniques. With the scaling of Al wiring, the spacing between metal lines has decreased to 50 nm or less. This means that the space for dry etching the 500 nm-thick Al has become 50 nm, resulting in an aspect ratio of 10:1, posing extreme difficulty. This has led to various serious defects, with the most common being Al undercut defects.

The defect occurs when etching extends from the bottom of the Al layer to the sidewalls, causing it to disconnect. The cause of this issue is that as the aspect ratio increases, the polymer, which serves to protect the Al sidewalls during dry etching, cannot effectively reach the bottommost part, resulting in etching. To overcome this, if the shape of the Al line is formed with a positive slope, it becomes highly susceptible to Al bridge defects.

Two methods were devised to overcome this, implemented in Samsung's 20 nm DRAM technology to confirm their effectiveness. Firstly, it was observed that Al undercut defects primarily concentrated at the edges of wafer. This is influenced by the temperature of the high chuck during dry etching, and it was found that precise temperature control was difficult with the current structure. Therefore, the chuck structure was modified from 2 zones to 4 zones to enable fine temperature adjustment, and the edge area was dry etched at a lower temperature to facilitate the transmission of more polymer.Secondly, the layout structure of the Al layer was reinforced. It was found that having discontinuous vulnerable patterns was more advantageous than continuously existing patterns. Therefore, irregular step patterns were created compared to patterns resembling hammers, and their effectiveness was confirmed.These two improvements were validated through test results of real 8G DDR4 products.

EM-ThP-3 Enhancing Electro-Physical Properties of DRAM Through Control of Silicon Diffusion in Titanium Nitride Based Barrier Layer, ***Jina Kim***, *Y. Kim,* Sungkyunkwan University, Korea

As DRAM cell sizes substantially scale down, silicon voids in CMOS gate electrode and memory cell bit-line connection nodes cause serious issues in DRAM performance. These voids are formed at the silicon-metal interface as a result of the each material's difference in diffusivity, where silicon atoms are sucked into the metal layer by the Kirkendall effect, and they are accelerated by heat. Due to the increase in the heat budget of subsequent processes to over 1000 degrees, innovative process for barrier metals preventing silicon diffusion becomes critically essential. In this study, we demonstrate the impact of silicon void defects through variations in thickness, composition, and other parameters of the Titanium silicon nitride (TSN) based barrier metal. To meet the higher barrier properties, TSN has been developed as multi-layer film structure of TiN/SiN, providing low resistance even at low thickness and with the ability to control the composition of Ti, Si and N to maximize barrier properties. Increasing the thickness of TSN can increase the diffusion path of Si, thereby reducing the frequency of Si void occurrence. Furthermore, by increasing the concentration of Si within TSN, it is possible to suppress TiN grain growth while promoting amorphization or the formation of fine grains, thereby inhibiting diffusion through grain boundary. We investigated the frequency of Silicon void occurrence before and after heat treatment using SEM/TEM, and confirmed the extent of improvements for each conditions. Finally, we have confirmed improvements in DRAM data write performance as resistance and short circuit decreased due to silicon void defects. Hereby we have provided a significant opportunity for the development of 10-nano-class DRAM.

EM-ThP-4 Integrating Molecular Photoswitch Memory with Nanoscale Optoelectronics, ***Nelia Zaiats***, *T. Kjellberg Jensen,* Lund University, Sweden

Using light for interconnectivity in artificial neural networks can be highly energy efficient and allow multiplexing. Important is the introduction of dynamic memory weights in these connections that can be integrated on-chip with nanophotonic components. We show that photochromic dyes, that reversibly switch their absorption of light, can be used as optical memories combined with highly efficient III-V nano-optoelectronics. We find that the dyes can be used for both short- and long-term memory by varying chemical and physical parameters of the sample, allowing to access a wide range of timescales. We demonstrate the effect both on individual nanostructures and arrays. We demonstrate the robustness over many switching cycles. Using the dye performance parameters, we find that it can function as the memory component in an anatomically verified model of the insect brain navigation complex. The work opens for artificial neural networks with energy-efficient light communication and on-chip molecular memory elements.

EM-ThP-5 Charge Trapping in a-Si_3N_4: Hydrogen as Savior and Saboteur, ***Lukas Hückmann***, *J. Cottom, J. Meyer,* Leiden University, The Netherlands

Amorphous silicon nitride (a-Si_3N_4) is an essential material for nanoelectronics due to its ability to trap charges, particularly in flash memory devices. EPR experiments combined with electronic structure calculations suggest that undercoordinated Si atoms (K-centers) are responsible for this phenomenon [1]. The propensity of such defects towards hydrogen passivation, however, raises the question of the completeness of this picture.

In this work, we combine simulations at force field (FF) up to hybrid density functional theory (DFT) level. Employing the MG2 force field [2], a comprehensive statistical ensemble of structural models for a-Si_3N_4 was generated through the melt-quench procedure, ensuring robust statistical significance in our analysis [3]. Adding charges to those models, we perform structural optimization using the HSE06 hybrid DFT-functional to ensure the localization of the band edges and defect trapping energies are well described. We identify a hitherto unknown mode of intrinsic polaronic

trapping of electrons in a-Si_3N_4: Charging can generate either a K-center or Si-Si-type defect. At the same time, discharging recovers the amorphous network's original structure [3]. Crucially, this study bridges the previously fragmented understanding of charge trapping and hydrogen incorporation. We demonstrate that hydrogen plays a dual role: It can repair coordination defects, healing the network, yet also promotes Si-N bond breaking in strained areas, thus compromising the network integrity [4]. Our findings offer a unified perspective on the interplay between defect formation, hydrogen behavior, and charge trapping, providing insights critical for optimizing a-Si_3N_4's electronic properties in nanoelectronic applications.

[1] Warren, W. L. et al.J. Appl. Phys.**1993**,*74*, 4034–4046.
[2] Marian, C. M.; Gastreich, M.; Gale, J. D.*Phys. Rev. B***2000**,62, 3117–3124.
[3] **Hückmann, L.**; Cottom, J.; Meyer, J.*Adv. Phys. Res*.**2024**,*3*, 2300109.
[4] Cottom, J.; **Hückmann, L.**; Olsson, E.; Meyer, J.*J. Phys. Chem. Lett.***2024**,*15*, 840–848,*Selected for cover*.

EM-ThP-6 Graded CdSexTe1-X /CdTe Thin-Film Solar Cells: In-Situ Dopant Profiling During Light Soaking, ***Sanghyun Lee,*** University of Kentucky*; K. Price,* Morehead State University

Cadmium Telluride (CdTe) thin-film solar cells have made significant progress in efficiency, with laboratory-scale tests surpassing 22.1%, edging closer to the theoretical Shockley-Queisser limit of around 32%. Recent research has been focused to integrate selenium (Se) into CdTe absorbers, creating band grading without CdS window layers. $CdSe_xTe_{1-x}$ is a prominent candidate to enhance the short-circuit-current (Jsc) by bandgap lowering below 1.45 eV. While CdS window layer intermixing mitigates the lattice mismatch, it concurrently limits absorbing light in the critical 300 - 525 nm range, resulting in efficiency loss. Thus, strategies to overcome this drawback have been focused on introducing Se to create band grading. $CdSe_xTe_{1-x}$ is promising, with bandgap lowering below 1.45 eV, pushing Jsc to their theoretical limit.

In this contribution, $CdSe_xTe_{1-x}$/CdTe devices were fabricated by vapor transport technology, and the mechanism of efficiency improvement was studied through in-situ Cu dopant profiling during light soaking. Moreover, devices were stressed at elevated temperatures simultaneously under various bias conditions, both with illumination and in the dark. The morphological and cross-sectional structure of the graded absorber were confirmed by Scanning Electron Microscopy and Electron Dispersive Spectroscopy. During light soaking, different intensities of light and temperatures were tested to characterize devices. Concurrently, we modeled the electronic structure of characterized devices using our in-house MATLAB modeling suites, connected to the external TCAD simulators, to explain the result with material and device input parameters. The results indicate that $CdSe_xTe_{1-x}$/CdTe devices have shallow donor and acceptor energy states near the main front junction interface. The concentration of Cu dopant is approximately 4 x 10^{14} cm^3 in the wake-up condition. The Cu dopant progresses toward the front $CdSe_xTe_{1-x}$ /CdTe junction during in-situ measurements.Interestingly, the stability of $CdSe_xTe_{1-x}$ solar cells was found to be bias-dependent and device-specific during light and dark soaking. $CdSe_xTe_{1-x}$ /CdTe devices without Cu dopant demonstrated depletion reduction width under light and dark-biased conditions. The depletion width of $CdSe_xTe_{1-x}$ devices without Cu is reduced to approximately 47 % under applied soaking conditions. Simultaneously, efficiency, Voc, and FF decreased, whereas Jsc show no clear dependency. Under light soaking conditions at 95 C, the increases in Voc, FF, and efficiency depend on light soaking conditions. The peak efficiency after 9 hr light soaking at 95 C is 12.90 %.

EM-ThP-7 Optimization of NiO Doping, Thickness, and Extension in Kv-Class NiO/Ga2O3 Vertical Rectifiers, ***Chao-Ching Chiang,*** *J. Li, H. Wan, F. Ren, S. Pearton,* University of Florida

We conducted a thorough analysis of vertical geometry NiO/Ga_2O_3 rectifiers using the Silvaco TCAD simulator to establish optimized breakdown voltages ranging from 1 to 7 kV. By manipulating key NiO parameters such as doping concentration (ranging from 10^{17} to 10^{19} cm^{-3}), thickness (ranging from 10 to 70 nm), and junction extension beyond the anode to form a guard ring (ranging from 0 to 30 µm), we determined the electric field distribution within each design. The factors of doping concentration, thickness, and junction extension were found to significantly influence the site of device breakdown, which could occur anywhere from the edge of the NiO extension to the edge of the top contact, consistent with experimental results. Further investigations also revealed varying breakdown voltages based on theoretical critical electric fields for different NiO bilayer thicknesses and doping concentrations.

EM-ThP-8 Theoretical Study of van der Waals Epitaxy of Bilayer Silicene on Iii-Sb Substrates, ***Kumar Vishal,*** *H. Huang, Y. Zhuang,* Wright State University

Research development of integrated silicon photonics in the mid-infrared (MIR) range has gained considerable momentum over the past decades, driven by its vital applications in biochemical sensing, medicine, and even astronomy communications. However, progress has been hampered by the limitation by the energy bandgap and optical transparency in conventional material. Very recently, it has been reported that 2D bilayer silicon (BLSi) demonstrates unique optical properties across the MIR spectrum. By adjusting the strain, the optical absorptions can be tuned in a wide range of wavelength from 1.5 -11.5 mm. However, experimentally the maximum in-plane strain achieved is ∼7% in a lattice-matching expitaxial silicon. Remote- and Van der Waals expitaxy methods can break the lattice-mismatch constraint to obtain single crystal 2D materials, but with an insufficient in-plane strain preserved in the 2D films.

In this work, motivated by the recent achievement of dative expitaxy of single crystalline Cr5Te8 on WSe2 enduring a ∼16% lattice mismatch, we conducted a theoretical study based on density function theory (DFT). Our aim is to explore the feasibility of growing BLSi on two III-Sb substrates: GaSb and AlSb. These substrates were chosen due to their ability to provide sufficient in-plane strain (11.92% and 12.23% respectively) to assure energy bandgap opening in BLSi. The generalized gradient approximation (GGA) and the strongly constrained and appropriately normed (SCAN) meta - generalized gradient approximation (meta-GGA) have been employed in the computation to analyze the chemical bond formation and to optimize the energetically favorable atomic structures. Our findings suggest that Van der Waals epitaxy of BLSi on both of the III-Sb substrates is viable when the substrate's surfaces are terminated with the metallic atoms. By forming the dative bonds between the BLSi and the III-Sb substrates, substantial in-plane strain in BLSi can be preserved, leading to a low buckled BLSi with an opened energy bandgaps.

EM-ThP-9 Low-Power, Highly Responsive Phototransistor Array Utilizing Plasma-Engineered Amorphous Metal Oxide Semiconductors, ***Uisik Jeong,*** *H. Rho,* Sungkyunkwan University, Korea*; S. Kim,* Sungkyunkwan University (SKKU), Republic of Korea

The potential for next-generation electronic applications is vast with the development of energy-efficient, high-performance broadband photodetectors using cost-effective amorphous metal oxide semiconductors.Commercially available photodetectors utilize various semiconductors to detect light across different wavelengths, from ultraviolet (UV) to near-infrared (NIR).However, the need for specific materials for different wavelengths limits their versatility. This study focuses on utilizing a metal oxide semiconductor, specifically indium gallium zinc oxide (IGZO), without the requirement for additional external photo absorption layers.Hydrogen (H_2) plasma treatment was employed to enhance charge carrier generation and create subgap states in the IGZO film, enabling wide-spectrum detection from UV to NIR without additional layers.Additionally, a ferroelectric and high-k dielectric were introduced as a gate dielectric to induce a high electric field on the channel, resulting in low-power operation.The H_2 plasma-treated IGZO phototransistors demonstrated ultra-high photoresponsivity (R ~ 10^3 AW^{-1}) and detectivity (D* ~ 10^{12} Jones) across abroad range of incident wavelengths (400 ~ 1000 nm), making them a promising candidate for next-generation optoelectronics.This study suggests a favorable method for the advancement of energy-efficient, cost effective, and high-performance broadband photodetectors.

EM-ThP-10 SOH Bake Time Optimization for SOH Void Reduction in Semiconductor Manufacturing, ***Jaehyeon Jeon,*** *B. Choi,* Sungkyunkwan University (SKKU), Republic of Korea

Spin-On Hardmask (SOH) materials are pivotal in semiconductor manufacturing for their superior masking quality, alignment accuracy, process control, and cost-effectiveness, crucial in patterning formation. However, insufficient chemical bonding between SOH and other layers, improper spin speed, or thickness can lead to void formation. In 10nm-scale DRAM products, where pattern sizes are extremely small, SOH voids can cause defects such as bridging and discontinuity in cell transistor gates. This paper demonstrates methods to minimize SOH void formation during the manufacturing process, focusing on the bake time. During SOH baking, condensation reactions and thermal degradation occur, leading to outgassing. In the early stages of baking, polymer condensation is prominent, and once cross-linking is complete, outgassing due to condensation diminishes. However, as bake time increases, outgassing due

to thermal degradation becomes more significant. Thus, minimizing void formation by reducing outgassing at the completion of condensation reactions can be observed, leading to improvements in defects such as bridging and discontinuity caused by SOH voids in final patterns.

EM-ThP-11 Synthesis of Lead free $KNbO_3$ Piezoelectric Film on $LiNbO_3$ Single Crystal by Hydrothermal Method, ***Thithi Lay***, *A. Hagiwara, R. Arai,* Josai University, Japan

Piezoelectric materials are in focus for many sensing applications such as vibrational sensors, pressure sensors, medical devices, wearable devices, energy harvesting devices, etc., [1-2]. Especially small scales energy harvester with clean energy sources is in demand for various portable electronics devices. Currently, the most widely used material for piezoelectric sensors is PZT because it has high piezoelectric properties compare to other. However, due to its Curie temperature the operating temperature of PZT is limited to 260℃ [5] and growing awareness of environmental hazard, lead free high temperature piezoelectric materials have been focus for new type of piezoelectric sensor [3]. To overcome with PZT in its piezoelectric properties, research and technology development are still in need and $KNbO_3$, $LiNbO_3$ and $LiTaO_3$ materials are consider as prominent candidates for lead free new and current device applications. Among them potassium niobate ($KNbO_3$) which has perovskite structure and curie temperature around 450℃ is receiving renewed interests because it has been found to exhibit high electromechanical coupling.

In this study well-ordered $KNbO_3$film were synthesis on $LiNbO_3$ single crystal substrate for the first time by hydrothermal method. Hydrothermal method has advantages in obtaining well-ordered thick film due to its reaction temperature which is possible under Curie temperature which is rather low compared to other method such as so-gel or aerosol deposition (AD) method. Crystal structure and film thickness were analyzed by SEM and XRD. $KNbO_3$ (100) and (111) structure epitaxially grown on $LiNbO_3$ (100) substrate. Grains size ranging from 1-7μm, and film thickness varies in 3-10μm. Experimental results with different reaction time showed that film thickness and grain size can be controlled by optimization of chemical reaction time in a single deposition process.

References

[1] Aussrine Bartasyte, Samuel Margueron, Thomas Baron, Stefania Oliveri, and Pascal Boulet, Toward High-Quality Epitaxial $LiNbO_3$, LiTaO3 Thin films for Acoustic and Optical Applications, Adv.Mater. Interfaces 4,160098-160998, 2017.

[2] Ryo Kudo, Peter Bornnann, Tobias Hemsel and Takeshi Morita, Thick $KNbO_3$ film deposited by ultrasonic-assisted hydrothermal method, acoust. Sci. & Tech. 36, 3262-264, 2015.

[3] T. Stevenson, D. G. Martin, P.I. Cowin, A. Blumfield, A. J. Bell, T. P. Domyn, P. M. Wearver, Piezoelectric materials for high temperatures transducers and actuators, J. Matter. Scpi. Mater Electron 26, 9256-9267, 2015.

EM-ThP-12 Thin Film Electrets Fabricated by Initiated Chemical Vapor Deposition (iCVD), ***Stefan Schröder***, *T. Hartig, L. Schwäke, T. Strunskus, F. Faupel,* Kiel University, Germany

Electrets are the electrostatic counterpart to permanent magnets, as they provide a (quasi-)permanent electric field. They have attracted great interest in the field of electronic applications ranging from sensors to energy harvesting. Polymers are usually selected as the starting material for the fabrication of stable electrets. New application pathways, e.g. in organic electronics, are increasing the demand for such materials in the form of thin films. Current wet-chemical polymer thin film fabrication is limited in the production of precise electret film thickness and dielectric breakdown strength. The reason for this are surface tension and dewetting effects in solution-based approaches as well as residual solvent molecules. This work highlights the fabrication of ultra-stable electret films by vapor phase deposition. Solvent-free, single-step initiated chemical vapor deposition (iCVD) is applied to fabricate precise polymer thin films of high dielectric breakdown strength on large-area substrates as well as complex geometries. Suitable material compositions are identified with the help of first principle calculations, based on electronic structure calculations. Furthermore, polarization effects are investigated, which result in long-term stability and precise tailoring of the iCVD electret surface potential. The fabricated films are tested in different electret transducers and show great potential for the application in next-generation devices.

EM-ThP-13 Interfacial Triangular Nanostructure Formation During Annealing of GaAsSb on InP, ***Leonid Miroshnik***, *D. Shima,* University of New Mexico*; A. Li,* University of Pennsylvania*; G. Balakrishnan,* University of New Mexico*; T. Sinno,* University of Pennsylvania*; S. Han,* University of New Mexico

Antimonide-based semiconductors (e.g., GaSb, InSb, AlSb) and their ternary/quaternary alloys are essential for high-operating temperature infrared devices, including thermal and photoelectric detectors, due to their narrow bandgaps which span the entire mid-wave infrared spectrum. However, the low melting points and chemical degradation modes of antimonide III-V materials pose significant manufacturing challenges when fabricating subsequent devices. In this work, we anneal epitaxial lattice-matched GaAsSb films grown on InP and capped with PECVD silicon nitride to show that atomic species rapidly diffuse across the heterojunction at temperatures as low as 675 °C. XRD and Raman analysis suggest the presence of Sb-rich and As-rich structures. Using TEM-EDX and geometric phase analysis, we show that antimony and indium diffuse across the epitaxial interface and create triangular structures composed of GaP faces with an InSb perimeter. The triangles range in height from 20 to 700 nm with an average height of 50 nm. Crystalline InSb nanostructures are observed at the tips of the triangles. These structures provide an opportunity for engineering the interface of antimony-based semiconductors and a potential method for the formation of confined InSb quantum structures. Furthermore, we discuss a mechanism in which this degradation mode may be enhanced or mitigated through film-strain engineering.

EM-ThP-14 Metal Matrix Composite Metallization Improves PV Module Efficiency and Electrical Bridging of Solar Cell Cracks for Durability, *A. Chavez,* University of New Mexico*; A. Jeffries,* Osazda Energy*;* ***Sang Han***, University of New Mexico*; S. Huneycutt, A. Ebong,* University of North Carolina at Charlotte*; D. Harwood, N. Azpiroz,* D2Solar*; B. White, B. Boyce,* Sandia National Laboratories

We have optimized the material properties of screen-printed, silver-carbon-nanotube-composite electrical contacts on Passivated Emitter and Rear Contact cells. We demonstrate that optimized carbon-nanotube-reinforced composite metallization increases ductility, fracture strength, and electrical cell-crack-bridging characteristics of gridlines over the conventional silver metallization. The fracture patterns, observed under *in situ* scanning electron microscope tensile tests, reveal that the increased ductility gives rise to much more pronounced slant fracture with an elongated metal overhang than the standard metallization. Finite element modeling is used to corroborate this observation. We visualize the plane stress condition near the crack tip, where the breakdown in triaxiality of stress leads to the slant fracture pattern. Tension test on individual gridlines, exfoliated from the substrate, further illustrates an increase in fracture toughness by a factor greater than 7x for the composite metallization, being consistent with the observation of pronounced overhang from the fractured gridlines. The improved ductility and fracture toughness ultimately result in electrical bridging of cell cracks wider than 65 μm. The composite metallization additionally provides a statistical increase in cell efficiency by 0.03%, full-sized module efficiency by 0.1%, and maximum power point by 1%, likely due to enhanced sintering of silver particles within the composite paste. We anticipate that our approach is easily translational to copper and aluminum pastes as well as recent cell technologies such as Tunnel Oxide Passivated Contact cells.

EM-ThP-15 Revisiting Materials from the B-C-N Family for Interconnect Dielectric Applications, ***Michelle Paquette***, *R. Bale, F. Berber Halmen, G. Bhattarai, S. Daneshmehr, S. Dhungana, M. Stoll,* University of Missouri-Kansas City

Fundamentally, the back-end interconnect system is made up of two material types: a metallic conductor, and an insulating dielectric. With the ongoing push for high-performance computing, the higher device and power density as well as speed requirements for integrated circuits place new and more challenging demands on these materials. As the semiconductor industry perseveres toward a replacement for the copper conductor, multiple different challenges face dielectrics, including more stringent deposition control, patterning flexibility, and property specifications (electrical, mechanical, thermal, etc). Boron-based solids have been considered as an alternative to silicon-based dielectrics due to their combination of potentially ultra-low dielectric constant with robust mechanical, electrical, and chemical properties. This contribution will cover recent advances and future potential for boron-based dielectrics from our group and others.

EM-ThP-16 Photoluminescence Measurements of Te-Doped Gasb from 10 K to 300 K Using FTIR Spectroscopy, *S. Yadav,* ***Sonam Yadav****, C. A. Armenta, J. R. Love,* New Mexico State University*; P. C. Grant,* University of Arkansas*; S. Zollner,* New Mexico State University

Gallium antimonide (GaSb) is a vital semiconductor for fabricating infrared optoelectronic devices, making it significant for next-generation infrared imaging systems. In this study, we investigated the photoluminescence (PL) properties of Te-doped GaSb with a doping level of 2 – 5 x 10^{17} cm^{-3}, across a temperature range from 10 K to 300 K using 400 mW laser power by using Fourier Transform Infrared Spectroscopy (FTIR) in the near IR spectral range. Our experimental results revealed that at room temperature, GaSb exhibits weak PL, which significantly increases as the temperature drops below 170 K. At 10 K, the PL intensity peaks sharply, corresponding to the direct band gap of 0.726 eV. As the temperature increases to 170 K, an additional peak emerges around 0.75 eV, which we attribute to the indirect recombination of L-valley electrons. We quantified the total number of electrons in both the L and Γ valleys, and the ratio of those enabling us to calculate the carrier concentration in each valley as a function of temperature. Our interest in GaSb PL stems from its analogous behavior to GeSn alloys with 10% Sn, making it a potential candidate for use in photodetectors. This work provides valuable insights into the temperature-dependent electronic properties of GaSb, highlighting its relevance in advanced optoelectronic applications.

EM-ThP-17 Atomic-Level Insights into RRAMs: Improving Performance and Energy Efficiency for Advanced Computing, *M. Chowdhury, A. Moazzeni,* ***Gozde Tutuncuoglu****,* Wayne State University

Conventional von-Neumann computing systems face significant limitations due to the memory-processor bottleneck, which restricts simultaneous data retrieval and instruction execution, leading to increased energy consumption and reduced performance. To surpass this bottleneck, next-generation computing devices must achieve substantial improvements in processing speed and energy efficiency. Emerging non-volatile memory technologies, such as resistive random access memories (RRAMs) based on crossbar arrays, offer a promising solution by integrating memory and computation, thereby enhancing computational efficiency and reducing energy usage.

In this talk, we will explore the resistive switching dynamics of non-volatile RRAM by analyzing their atomic and electronic structures. Our focus will be on transition metal oxide RRAMs fabricated using DC-sputtering and Atomic Layer Deposition (ALD) techniques, known for their high performance and compatibility with CMOS technology. We aim to provide detailed insights into how materials properties, such as stoichiometry, affect device performance metrics and how these properties can be modified using data-guided experimental techniques.

Our research objectives center on capturing the intricate details of these structures to optimize the performance of RRAM devices. By leveraging atomic-level insights, we aim to tailor these devices to meet the specific requirements of various computing algorithms. This optimization will be guided by advanced device-to-algorithm benchmarking tools, facilitating a comprehensive analysis linking the atomic and electronic properties of RRAMs to their overall performance in computational applications.

Through this approach, we expect to provide materials-focused pathways to enhance the efficiency and reliability of RRAMs, thereby making them a more viable option for future in-memory computing technologies. This talk will contribute to the fundamental understanding of RRAMs and present practical solutions for optimizing their use in advanced computing systems.

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