2D Materials Technical Group
Room C123 - Session 2D+EM-FrM

2D-Materials: Device Application

Moderators: Maria Hilse, Pennsylvania State University, **Tongcang Li**, Purdue University

8:20am **2D+EM-FrM-1 Stochastic Computing Enabled by 2D Memtransistors*, Saptarshi Das,*** Pennsylvania State University **INVITED**

In the emerging era of artificial intelligence, deep learning, and Big-data, the energy and hardware investments required for conventional high-precision digital computing are becoming increasingly unsustainable. As a result, there is a growing need for a new paradigm that prioritizes energy and resource efficiency over precision for many computing applications. Stochastic computing (SC) is a promising alternative because it can perform basic arithmetic operations using simple logic gates, unlike digital computers that require many logic gates and a high transistor volume. However, the hardware investment necessary to generate stochastic bits (s-bit), the fundamental computing primitive for SC, has hindered its widespread adoption. While traditional silicon complementary metal oxide semiconductor (CMOS) technology can accelerate SC, it still requires extensive hardware investment. Memristor and spin-based devices offer natural randomness but rely on hybrid designs involving CMOS peripherals, which increase the area and energy burden.

To overcome these limitations, we have developed a standalone SC architecture embedded in memory based on two-dimensional (2D) memtransistors. This monolithic and non-von Neumann SC architecture requires only a tiny amount of energy (< 1 nano Joules) for s-bit generation and to perform arithmetic operations, and occupies a small hardware footprint, highlighting the benefits of SC. Additionally, the researchers demonstrate the acceleration of Bayesian inference using their SC platform.

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9:00am **2D+EM-FrM-3 Electrical Characteristics of Semi-Metallic 2H-$NbSe_2$ for Scalable Interconnects*, Abir Hasan,*** *T. Alem, C. Rogers, S. Stevenson, S. McDonnell, N. Shukla,* University of Virginia

Despite Copper being the current material of choice for interconnect technology, it suffers from increased resistivity at scaled dimensions and the necessity for a barrier-liner to prevent diffusion. This has motivated the exploration of alternate materials that can overcome these limitations for scaled CMOS technology nodes. Metallic 2D materials can offer a promising option. In this work, we evaluate the properties of 2D semi-metallic material 2H Niobium diselenide (2H-NbSe2) as a candidate for realizing highly scalable interconnect technology without the need for barrier-liner. We performed detailed electrical characterization evaluating the dimensional scaling, dependence of the resistivity on temperature, device lifetime, effect of encapsulation layer etc. on ribbon devices fabricated with 2H-$NbSe_2$ material. 2H-$NbSe_2$ showed negligible change in resistivity compared to the bulk value when scaled down to thicknesses less than 15 nm. High current density transport measurements are performed on 2H-$NbSe_2$ ribbon devices with varied width (0.1-1um) at elevated temperature (>= 100^{o}C) to assess the reliability and failure characteristics. Lifetime of the $NbSe_2$ ribbons improved when an Al_2O_3 encapsulation layer was used. Our work provides critical insights into the potential of $NbSe_2$ for realizing scalable interconnects.

9:20am **2D+EM-FrM-4 Magneto-Transport Measurement and Maximum Entropy Mobility Spectrum Analysis in Semiconductor Substrates for Graphene Growth*, Ruhin Chowdhury,*** University of New Mexico*; A. Majee,* Intel Corp.*; E. Renteria, D. Ghosal,* University of New Mexico*; M. Arnold, M. Lagally,* University of Wisconsin - Madison*; F. Cavallo,* University of New Mexico

Our study focuses on the multi-carrier electrical transport characterization of heat-treated bulk Ge near its melting point. Single-crystalline Ge has recently gained relevance as a substrate for the chemical vapor deposition (CVD) of high-quality graphene sheets, nanowires, and nanoscale wigglers.[1,2] Deposition of graphene on (110) Ge substrates allows integration of a 2D sheet with widely used semiconductors without the need for release and transfer processes, which may lead to the degradation of graphene's structural and functional properties. Determining the full potential of graphene/Ge for electronic applications requires understanding charge transport in this material combination. To date, quantitative models of lateral charge transport in graphene/Ge (i.e., transport of mobile carriers in the direction parallel to the graphene/Ge interface) are not available, primarily due to the overwhelming contribution of bulk Ge. In this work, we isolated and identified all mobile carrier types undergoing drift in heat-treated Ge at the typical condition for CVD of monolayer graphene. We believe these results to be the basis for quantifying carrier mobilities, carrier concentrations, and carrier types in graphene/Ge.

We performed magneto-transport measurements of heat-treated Ge between 50 K and 400 K and a magnetic field spanning from -7T to 7T to extract the conductivity tensor of the material. The Ge substrates were nominally intrinsic before annealing. Next, we used maximum entropy mobility spectrum analysis (MEMSA)[3] to identify the carrier types contributing to transport in Ge (110). Our analysis consistently shows the contribution of heavy holes (HH) and light holes (LH) in bulk Ge. The excess holes in bulk Ge are attributed to the formation of acceptor-like vacancies during high-temperature annealing of Ge.[4] The trend of carrier mobility vs. temperature indicates that different scattering mechanisms are dominant for HH and LH in a given temperature range. In addition to the contribution of HH and LH in bulk Ge, we identified two additional carrier types, namely electron and ultra-low mobility holes. We attribute the electrons to donor-type interstitials and the low-mobility holes to accumulated HH near the native oxide/Ge interface.

ACKNOWLEDGMENT. This work was supported by the U.S. AFOSR and Clarkson Aerospace Corporation under award No. FA9550-21-1-0460/UNM 21-1-0460.

[1] B. Kiraly, et al. Nano Lett. 15, 11, 7414–7420 (2015)

[2] R.M. Jacobberger et al. Nat. Commun. 6, 8006 (2015)

[3] Kiatgamolchai, S., et al. Phys Rev E Stat Nonlin Soft Matter Phys 66(3 Pt 2B): 036705 (2002)

[4] S. Mayburg, Phys. Rev. 95, 38 (1954).

9:40am **2D+EM-FrM-5 What Are 2D Materials Good for?*, E. Pop, Tara Pena,*** Stanford University **INVITED**

This talk will present my (biased!) perspective of what two-dimensional (2D) materials could be good for. For example, they could be good for applications where their ultrathin nature gives them distinct advantages, such as flexible electronics [1] or light-weight solar cells [2]. They may not be good where conventional materials work sufficiently well, like transistors thicker than a few nanometers. I will focus on 2D materials for 3D heterogeneous integration of electronics, which presents major advantages for energy-efficient computing [3]. Here, 2D materials could be monolayer transistors with ultralow leakage [4] (due to larger band gaps than silicon), used to access high-density memory [5]. Recent results from our group [6,7] and others [8] have shown monolayer transistors with good performance, which cannot be achieved with sub-nanometer thin conventional semiconductors, and the 2D performance could be further boosted by strain [9]. I will also describe some unconventional applications, using 2D materials as thermal insulators [10], heat spreaders [11], and thermal transistors [12]. These could enable control of heat in “thermal circuits” analogous with electrical circuits. Combined, these studies reveal fundamental limits and some unusual applications of 2D materials, which take advantage of their unique properties.

Refs: [1]A. Daus et al., Nat. Elec. 4, 495 (2021).**[2]** K. Nassiri Nazif, et al., Nat. Comm. 12, 7034 (2021). **[3]** M. Aly et al., Computer 48, 24 (2015). **[4]**

C. Bailey et al., EMC (2019). **[5]** A. Khan et al. Science 373, 1243 (2021). **[6]** C. English et al., IEDM, Dec 2016. **[7]** C. McClellan et al. ACS Nano 15, 1587 (2021). **[8]** S. Das et al., Nat. Elec. 4, 786 (2021). **[9]** I Datye et al., Nano Lett. 22, 8052 (2022). **[10]** S. Vaziri et al., Science Adv. 5, eaax1325 (2019). **[11]** C. Koroglu & E. Pop, IEEE Elec. Dev. Lett. 44, 496 (2023). **[12]** M. Chen et al., 2D Mater. 8, 035055 (2021).

10:40am **2D+EM-FrM-8 Effect of Temperature on the Surface Morphologies of Sulfurized-Grown WS_2,** ***Md Samim Reza****, M. Singh,* Indian Institute of Technology Delhi, India

Tailored morphologies are essential for realizing the diverse applications of tungsten disulfide. This work reports on a successful growth of WS_2 that involves the sulfurization of a sputter-deposited (Angstrom Engineering Evovac) thin film of tungsten (150-300 Å with a rate of 0.4 Å/s) on a SiO_2 substrate (University Wafers) and the effect of temperature on the surface morphology of as-grown WS_2. The as-deposited tungsten substrate was cut into 2cm x 2cm and placed inside a custom-design horizontal CVD system (Quazar Technologies). A sulfur (99.5% pure precipitated powder, 600-1000 mg, Sigma Aldrich) was placed upstream (20-40 cm) from the tungsten heating zone (700-1000 °C) to grow WS_2 under a carrier gas (Ar) flow of 0-400 sccm. Raman spectroscopy (514 nm laser source with a spot size of ~1 um^2 for 100x objective, 1mW power, Renishaw inVia) revealed the peaks at ~350/cm and ~417/cm, confirmed the growth of WS_2 and the peak intensity ratio of in-plane and out-of-plane ($E^1{}_{2g}/A^{1g}$) < 1, suggest a multilayer growth [1]. The X-ray diffraction (Rigaku Ultima IV) analysis indicates the growth of hexagonal-phased WS_2 (JCPDS: 08-0237) with a mixed plane to a (002)-dominated at higher temperatures. The field emission scanning electron microscopy (Magna LMU, Tescan) scans revealed the growth morphology from a planar to a nanoflower, forming a thin film of WS_2. Different sulfurization temperatures result in distinct morphologies, with a thin film morphology obtained at 700-750°C, followed by the dominance of nanoflower-like WS_2 structures between 850°C and 950°C as observed by field emission scanning electron microscopy. At temperatures higher than 950°C, WS_2 nanoflowers with vertical alignment are grown on a SiO_2 substrate. Electron dispersive X-ray (EDX, Ametek) spectra show a stoichiometry close to 1:2 for W: S. The atomic force microscope analysis (Dimension Icon, Bruker) revealed that surface roughness (sputter-deposited tungsten roughness of ~80 pm) increased from ~5 to 80 nm with the growth temperature. The experimental results emphasize the importance of temperature in determining the surface morphologies of WS_2. The ability to control the growth temperature offers customization of WS_2 morphologies that could allow the fabrication of WS_2-based devices with the desired properties [2-3].

[1] Berkdemir et al., Scientific Reports, 3, 1755 (2013)

[2] Sebastian et al., Nature Communications 12, 693 (2021)

[3] Li et al., The Journal of Physical Chemistry C, 126(22), 9293-9303.

11:00am **2D+EM-FrM-9 The Study of Internal Ion Transport in Ionic $CuInP_2S_6$,** ***Yujie Sun****, B. Liu,* Tsinghua University, China

Memristor-based neuromorphic computing is promising for artificial intelligence. However, most of the reported memristors have limited linear computing states and consume large operation energy which hinder their applications. Herein, we report a memristor based on ionic two-dimensional $CuInP_2S_6$ (2D CIPS), in which up to 1350 linear conductance states are achieved by controlling the migration of internal Cu ions in CIPS. In addition, the device shows a low operation current of ~100 pA. Cu ions are proven to move along the electric field by *in-situ* scanning electron microscopy and energy dispersive spectroscopy measurements. Furthermore, complex signal transport among multiple neurons in the brain is imitated by 2D CIPS-based memristor arrays. Our results offer a new platform to fabricate high-performance memristors based on ion transport in 2D materials for neuromorphic computing.

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