Electronic Materials and Photonics Division
Room B116 - Session EM1+TF-FrM

Advanced Patterning and Fabrication for Device Scaling

Moderators: Stephen McDonnell, University of Virginia, **Michelle Paquette**, University of Missouri-Kansas City

8:20am **EM1+TF-FrM-1 Thin Film Challenges and Opportunities in a 3D-Evolving Memory Landscape***, **Johan Swerts,*** imec, Belgium **INVITED**

Device architectures used in SRAM memory transitioned in the past decade from the historical 2D planar transistor to FINFET. The next innovation revealed for the 3nm node is a 3D stacked gate-all-around architecture in combination with a backside power delivery network. For further scaling, stacking nmos and pmos, the so-called complementary-FET (CFET) design, is envisaged to happen in 2030. New metallization schemes to tackle the RC challenge as device dimensions of the interconnects shrink, such as Cu replacements materials in a direct metal etch integration scheme. A broad variety of complementary deposition techniques and introduction of new materials will be needed to enable the above-mentioned novelties.

A similar trend towards stacking functional cells can be observed in various memories, such as the emerging memories that aim to bridge the gap between DRAM and NAND, thereby enabling fast data storage and retreival for real-time processing in connected devices at low cost. These memories are based on phase change, filamentary, magnetic, or ferroelectric mechanisms and often use multi-element materials. They have been extensively explored in 2D capacitor or transistor based devices, but for further density scaling 3D device designs are needed where a conformal deposition technique such as ALD is required. Cell scaling challenges also hold for the traditional DRAM which lead to exploring 3DDRAM integration routes. One viable pathway for scaling implies the replacement of the typical Si-channel based transistor by a deposited semiconductor oxide channel. Ultimate 3DDRAM implementation would require a conformal deposition of that channel.

This presentation reviews key thin film opportunities and challenges, including but not limited to ALD, in a 3D-evolving memory landscape.

9:00am **EM1+TF-FrM-3 Patterning Challenges in the Era of Vertical Scaling***, **Luciana Meli,*** IBM Research Division, Albany, NY **INVITED**

With the end of conventional device scaling, achieving higher compute power has relied on a combination of design and integration innovations, and material breakthroughs to keep up with scaling demands. While traditional dimensional scaling will only continue for the back end of the line, controlling pattern variability and placement remains a critical challenge from a lithography perspective.

Looking ahead, vertical scaling paths will be essential to enhance performance in traditional analog computing and to scale up qubits in quantum computing. This talk will focus on key patterning challenges associated with these vertical scaling pathways, including stacked FETs and chiplet-based architectures, and address opportunities for innovation.

9:40am **EM1+TF-FrM-5 Plasma Etch Challenges and Innovations to Enable sub-26nm Pitch L/S Patterning with High-NA EUV***, **Nafees Kabir,*** Intel Corporation

Extreme ultraviolet (EUV) lithography has been a game changer for the semiconductor industry, enabling tight pitches of 36-40 nm for the 7nm logic technology node. Employing an extremely short 13.5nm wavelength, EUV lithography has surpassed 193i by improving resolution and thus the ability to print tighter features, as well as replacing the complex and expensive multiple-step patterning of 193i with single-patterning. However, despite achieving single-exposure 28nm pitch for the 5nm logic technology node, the current scanner is approaching its resolution limit.

As we prepare to embrace another litho evolution, **high-NA EUV lithography technology**is projected to enable 2nm and beyond logic technology nodes without requiring complex multi-step patterning. The key enabler to improve resolution is the numerical aperture (NA) of the lens. Hence, moving from current **0.33NA to 0.55NA** has the ultimate capability to enable 8nm resolution and patterning 16nm pitch with single-exposure. With this change in NA, the depth-of-focus (DOF) is reduced and pushes us towards the use of **thinner resists** (~20-25nm FT).

This brings us to a new process territory, not only for litho, but also for plasma etch. Need for etch innovation is at a premium to work hand-in-hand to enable pattern transfer of critical features in beyond-2nm logic nodes to further advance Moore's Law.

In this work, we will share some early innovative plasma etch techniques to demonstrate patterning of basic elements like lines/spaces, contact holes etc. and novel process integration schemes involving Chemically Amplified Resists (CAR) to enable more complex structures with high fidelity.

10:00am **EM1+TF-FrM-6 Area-Selective Deposition with Carborane and Aromatic Self-Assembled Monolayer Blocking Layers***, **Michelle Paquette**, R. Bale,* University of Missouri-Kansas City*; B. Garland,* Lehigh University*; S. King,* Intel Corporation*; A. Molder, N. Oyler, S. Pinnepalli,* University of Missouri-Kansas City*; N. Strandwitz, V. Vemuri,* Lehigh University*; T. Vo,* University of Missouri-Kansas City

Area-selective deposition (ASD) is an important strategy in improving the fidelity of and/or reducing the complexity of current multi-pattern pitch-division processes. Dielectric on dielectric (DoD) deposition is of interest for fully self-aligned via flow; however known DoD processes are limited in terms of materials, selectivities, and processing ranges. A common strategy for achieving ASD is to use a blocking layer on the non-growth surface (e.g., a metal) to be able to deposit a target material selectively on the desired surface (e.g., a dielectric). The most well-established blocking layers are self-assembled monolayers (SAMs) based on long alkyl chains, such as dodecanethiol. While these have demonstrated extremely promising results, they do present limitations such as restricted processing windows (e.g., temperature), a typical requirement for solution-phase processing, long exposure times (e.g., 12–48 h), limited stability (temperature, time, chemical), and presence of defects (e.g., pinholes) resulting from disorder or alkyl chain distortions. We investigate two alternative classes of SAMs as blocking layers on metal: carborane thiols and aromatic thiols. Both classes possess several appealing features including the capacity for well-ordered packing (based on 3D symmetry and Van der Waals packing for carboranes and pi-stacking for aromatics), vapor phase deposition, and—importantly—cross-linking through a variety of mechanisms including heat, plasma, and radiation (e.g., UV, e-beam), thus potentially enabling fewer defects, greater stability (leading to wider/more flexible processing windows and/or higher selectivity), as well as the possibility of additional top-down patterning. We investigate the influence of SAM formation (substrate, derivative, deposition conditions, post-deposition treatment) on their resulting composition and structure as well as their blocking capability toward a selection of atomic layer deposition chemistries.

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