Plasma Science and Technology Division
Room A106 - Session PS+TF-MoM
Plasma Processing for Advanced Emerging Memory Technologies

Moderators: Harutyun Melikyan, Micron Technology, **Jeffrey Shearer**, TEL

8:20am **PS+TF-MoM-1 IBE Patterning and Characterization of High Density STT-MRAM at Pitch 50nm and MTJ CD 20nm***, **Romuald Blanc**, L. Souriau, K. Wostyn, S. Couet, F. Lazzarino,* IMEC, Belgium

Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) is a promising non-volatile memory technology that offers high-density storage, low power consumption, and fast read/write operations. One potential application of STT-MRAM is as a last level cache (LLC) in computer systems, since it can offer higher performance, lower power consumption, and higher scaling potential than traditional SRAM. However, the patterning of STT-MRAM with Ion Beam Etching (IBE) at CD 20nm and pitch 50nm presents several challenges such as high aspect ratio, damaged magnetic-tunneling junction (MTJ) and sidewall shorts[1,2]. IBE relies on physical ion sputtering which does not allow high selectivity to the hard mask, therefore the choice of the hard mask stack is crucial to avoid excessively high aspect ratio[3]. In this study, we use a hybrid hard mask composed of high-density diamond-like carbon (DLC) to increase etch selectivity and TiN which becomes the STT-RAM top electrode.

In this talk, we present the magnetic and electrical results obtained for STT-MRAM at pitch 50nm using multiple process conditions of IBE main etch, sidewall clean and post-oxidation. We demonstrate that the etch parameters have a significant impact on device yield, with the best condition leading to a wafer-level yield of 95% functional devices with Tunnel Magnetoresistance (TMR) higher than 100%. On the best devices, we measure a TMR of 170% which corresponds to the TMR value before MTJ patterning. Finally, we report a switching current of 20µA with low dependence on pulse width from 5 to 20ns which is consistent with a MTJ CD of 20nm.

References:

[1] Lei Wan et al, *Fabrication and Individual Addressing of STT-MRAM Bit Array With 50 nm Full Pitch*, IEEE TRANSACTIONS ON MAGNETICS, VOL. 58, NO. 5, MAY 2022

[2] Murat Pak et al, *Orthogonal Array Pillar Process Development for High Density 4F2 Memory Cells at 40nm Pitch and Beyond*, SPIE Advanced Lithography 2022, Paper 12051-45

[3] Kuniaki Sugiura et al, *Ion Beam Etching Technology for High-Density Spin Transfer Torque Magnetic Random Access Memory*, Japanese Journal of Applied Physics 48 (2009) 08HD02

8:40am **PS+TF-MoM-2 Cryogenic Etching by Physisorption of Neutrals for High-Aspect-Ratio Contact***, **Masahiko Yokoi**, R. Suda, K. Tanaka, M. Tomura, K. Matsushima, Y. Ohya, M. Honda, Y. Kihara,* Tokyo Electron Miyagi Limited, Japan

The most crucial challenge in High-Aspect-Ratio (HAR) dielectric etching is supplying both ions and etchants [1] at the same rate to the etch front. If a large amount of etchant supplied to bottom of the feature is consumed by sufficient ion bombardment, higher aspect ratio etching with superior etching rate can be achieved. Conventional HAR processes which rely on the formation of radicals utilize fluorocarbon and hydrofluorocarbon gases combined with high-applied bias power. However, the stable chemisorption of radicals on feature sidewalls decreases the radical flux at the etch front, which results in a lack of radical supply and a drastic etch rate attenuation in the high aspect region. A technological breakthrough has long been required to solve this problem.

In this work, we focus on neutral physisorption at cryogenic temperatures. There have been several reports on plasma etching in the cryogenic temperature regime [2, 3], but the mechanism has not yet been well understood nor implemented for HAR dielectric etching. We have evaluated a novel etchant in cryogenic temperature and discovered a synergy between hydrogen fluoride (HF) as the etchant and HAR etching process. The dielectric etch rate strongly correlates with the physisorption of the HF, enhanced in the cryogenic temperature regime. The direct injection of HF as the process gas yields higher partial pressure and increased flux compared to radical flux formed by plasma reaction in vapor phase. Furthermore, we confirmed that the phosphorous-containing gas acts as an effective catalyst in the HF reaction. The phosphorous-containing gas stabilizes the HF or etchant physisorption on the SiO_2 film, which provides an etch rate enhancement at cryogenic temperature. In this conference, we will present a detailed surface reaction model.

Applying this innovative process to HAR etching enables a higher etch rate, higher selectivity, and higher aspect ratio etching capability. This novel process will enable the manufacturing of next-generation 3D NAND flash memory devices.

[1] K. Ishikawa, et al., Jpn. J. Appl. Phys. Vol. 57, No. 6S2, 06JA01, (2018).

[2] T. Ohiwa, et al., Jpn. J. Appl. Phys. Vol. 31, p.405, (1992).

[3] R. Dussart, et al., J. Phys. D: 47123001, (2014).

9:00am **PS+TF-MoM-3 Plasma Etching Processes Challenges in Emerging Non-Volatile Memories***, C. Boixaderas, T. Magis, C. Socquet, A. Roman, B. Martin,* CEA-LETI, France*; B. Fontaine, P. Gouraud,* STMicroelectronics, France*; J. Dubois,* STMicrolectronics, France*; N. Posseme,* STMicroelectronics, France*; L. Grenouillet, C. Jahan, G. Navarro, G. Bourgeois, M. Cyrille, **Thierry Chevolleau**,* CEA-LETI, France **INVITED**

Since the appearance of flash memory in 1980s, the non-volatile memory (NVM) market is in constant evolution. Nowadays the random access memory (RAM) market is divided into two categories: standalone memories and embedded memories that are integrated into the core CMOS.Since the 2010s, new non-volatile embedded memories are emerging to achieve specific performances in terms of storage, speed, endurance and retention. Such advanced memories are based on resistive (RRAM), material phase change (PCRAM), magnetic (MRAM) and ferroelectric (FeRAM) properties. An overview of the main advanced memory technologies will be presented (operation principles, materials and investigated multilayers stacks).

We will address the patterning challenges that we are facing for the integration of the advanced non-volatile memories. We will mainly focus on the etching and stripping development in terms of scaling down, profile control and plasma induced damages on features sidewalls. The etch process optimization to control the profile and potential technological solutions to minimize plasma damages will be also presented and discussed in terms of plasma surface-interaction.

9:40am **PS+TF-MoM-5 Principle and Application of Etching Lag Mitigation in High Aspect Ratio Contact Process***, **Kyoungsoo Chung**, H. Kim, S. Park, J. Min, K. Yoon, B. Kuh,* Samsung Electronics, Republic of Korea

High Aspect Ratio Contact (HARC) etching is associated with various defects, such as random bending, global tilting, hole distortion, and vertical CD reduction. Depth loading, in particular, is significant and is intricately linked to all these issues. The implementation of a cryogenic process with specific gases has been verified to increase the initial etch rate by nearly threefold compared to the high-temperature process. Furthermore, this procedure has also amplified the patterned aspect ratio where etching lag is observable, in addition to increasing the etch rate. We engage in a comprehensive review and investigation of the mechanisms contributing to the improvement of etching lag. Firstly, it is essential to attain a substantial physisorption amount of neutrals, including radicals, while concurrently delivering highly directional ion energy to activate the surface. Additionally, the transport of neutrals within the hole is crucial for the etchant to be effectively adsorbed up to the etch front. We argue that elements such as a cryogenic environment, low-molecular-weight etchants, compounds that facilitate surface reactions, and a distribution of highly energetic ions are vital for overcoming depth loading. Ultimately, we propose advanced strategies for next-generation HARC etching, based on the lag reduction mechanisms.

10:00am **PS+TF-MoM-6 Etching Selectivities of SiO_2 and SiN Against *a*-C Films Using CF_4/H_2 with a Pseudo-Wet Plasma Etching Mechanism*, Yusuke Imai*,** *S. Hsiao, M. Sekine, T. Tsutsumi, K. Ishikawa,* Nagoya University, Japan*; M. Iwata, M. Tamura,* Tokyo Electron Ltd., Japan*; Y. Iijima,* tokyo Electron, Japan*; T. Gohira, K. Matsushima, Y. Ohya,* Tokyo Electron Ltd., Japan*; M. Hori,* Nagoya University, Japan

With the advancement of cloud computing and AI technology, there is a growing demand for high-speed processing of large amounts of data and high-capacity storage. To manufacture 3D NAND, it is necessary to etch the layer structure where SiO_2 and SiN layers are alternately stacked, utilizing the amorphous C layer as a mask. A continuous increase of interest using cryogenic etching for high aspect ratio structure can be observed. Recently, etch selectivities among SiO_2, SiN and poly-Si with CHF_3/Ar and an ultra-high speed etch process at cryogenic temperature for 3D NAND have also been reported.[1,2] However, the cryogenic etching on variation of selectivities among SiN and SiO_2 over a-C have not been discussed yet. In this study, the etching selectivity among SiO_2, SiN and a-C was investigated by varying the hydrogen content (20 to 60 %) in CF_4/H_2 plasma at substrate temperature (T_s) of -60 and 20 °C. A capacitively coupled plasma reactor was used in the experiments, The total flow rate of gas mixture of CF_4 and H_2 was set at 150 sccm and the pressure during process was fixed at 4 Pa. As shown in the supplementary file, at T_s = 20 °C, the both ER of SiO_2 and SiN films decreased with increasing the hydrogen content, which is consistent with previous studies. Contrarily, for T_s = -60 °C the ER of SiO_2 reached its maximum at around 30-40% hydrogen additives, while the ER value of SiN decreased by nearly half compared to that at 20 °C. As a consequence, the etching selectivity of SiO_2/SiN at 20 °C was found to be less than 1 for all hydrogen contents, indicating that SiN was preferentially etched. For T_s = -60 °C it exhibited values greater than unity with the same process. This demonstrates that surface reactions and etching mechanism were changed when substrate was cooled. On the other hand, for *a*-C films increasing the hydrogen content in the CF_4/H_2 plasma results in a transition from etching to deposition. The transition point was found to be H_2 additive of around 50% at 20 °C and around 30% at -60 °C, indicating a wider process window with infinite etching selectivities of SiO_2/SiN over *a*-C mask at low T_s. The etching characteristics at low temperature is correlated to the surface reactions between the films and neutral HF, based on the results of HF molecular density during plasma discharge using FTIR. A pseudo-wet etching mechanism was proposed to explain the obtained results. The bias power was also varied to investigate the etching behavior further at cryogenic temperature.

[1] R. Dussart *et.al.*, J. Appl. Phys. **133**, 113306 (2023).

[2] Y. Kihara *etal*., VLSI symposium T3-2 (2023)

10:40am **PS+TF-MoM-8 Enhancing Etching Processes at Lower Wafer Temperatures: New Insights into Chemical and Physical Mechanisms*, Thorsten Lill,*** Clarycon Nanotechnology Research, Inc. **INVITED**

Lower temperatures hold significant importance for etching advanced memory devices. In this presentation, we provide a comprehensive overview of the chemical and physical processes involved in etching at lower wafer temperatures. Traditionally, plasma etching techniques heavily rely on the generation of radicals that readily chemisorb onto the surface. However, at low temperatures, molecules tend to adsorb through physisorption, lacking the necessary energy to overcome the energy barrier required for a chemical reaction. However, the concentration of neutrals in typical plasma used for semiconductor manufacturing is notably higher (by one to two orders of magnitude) than that of radicals. At lower temperatures, the physisorption of neutrals becomes significant, increasing their concentration on the surface and contributing to the etching process once chemically activated by energy from the plasma [1].

Etching of high aspect ratio structures utilizes ions and neutral reactive species that must effectively traverse through high aspect ratio features to reach the etch front. We present computational results on neutral transport within such features, exploring the influence of aspect ratio, profile shape, and surface processes including adsorption, desorption, and diffusion of neutral species. Our findings indicate a substantial increase in the steady-state transmission probability with the introduction of surface diffusion [2]. While spontaneous and collision-induced desorption of adsorbed neutrals alone do not alter the steady-state transmission probability, they do impact the time required to reach it. However, in the presence of surface diffusion, spontaneous desorption enhances the transmission probability, whereas desorption resulting from collisions with co-flowing nonreactive gas reduces it. These results unveil the potential for enhancing neutral transport at low surface temperatures, facilitated by physisorption and surface diffusion mechanisms.

By shedding light on the intricate interplay between chemical and physical phenomena during etching processes at lower temperatures, this presentation provides insights into the optimization of etching techniques for advanced memory devices.

[1]T. Lill, I. L. Berry, M. Shen, J. Hoang, A. Fischer, T. Panagopoulos, J. P. Chang, and V. Vahedi, J. Vac. Sci. Technol. A 41, 023005 (2023).

[2]T. Panagopoulos, T. Lill, J. Vac. Sci. Technol. A 41, 033006 (2023)

11:20am **PS+TF-MoM-10 High Selectivity Etching via Pulsed Selective Deposition*, André Amend,*** *M. Yakushiji, K. Kuwahara,* Hitachi High-Tech, Japan

Semiconductor device structures are shrinking and increasing in verticality, thus requiring novel plasma dry-etching processes to manufacture high Aspect-Ratio (AR) profiles on nanometer scales. Fabrication of such devices requires hard masks (HM) with high etching resistance that have small Critical Dimension (CD) and large height, corresponding to the needs of the device dimensions. As a result, creating the HMs themselves becomes more expensive and requires costly multi-layer processes to deal with the relatively low etching resistance of the C-rich photomask, which transfers the device pattern via photolithography. HM fabrication could be significantly simplified by an etching process that selectively etches hard materials, such as SiO_2, even under soft C-rich masks.

Here, a Phase Mask Reconstruction Process (P-MRP) is introduced, that drastically increases the SiO_2 etching selectivity and is compatible with small CD structures. P-MRP allows control of the C-based mask shape while etching SiO_2 via a time-modulated bias voltage, that tunes separate selective mask deposition and sample etching phases with a frequency up to above 1000 Hz. While a high voltage is applied to the sample, high-energy ions promote etching, whereas deposition occurs during the low voltage phase. Preferential deposition on the mask is achieved via chemical selectivity and radical shading due to the mask AR.

By precise control of the time-modulated sample bias voltage to adjust etching and deposition phases, the etching selectivity, as well as the mask shape and stability, can be controlled, which is critical to processing small patterns. To achieve high selectivity, the net etching rate on top of the mask can be decreased by reducing average ion energy, while controlling the mask side-deposition rate via the maximum ion energy and duration of the deposition phase. Since P-MRP rapidly alternates mask etching and mask passivation (during the deposition phases) low pattern roughness is achieved as well. For Line/Space and Hole patterns with CD 16-26 nm, etching selectivity as high as 10 was demonstrated while etching a depth of up to 200 nm of SiO_2, with AR of up to about 10.

This result indicates that P-MRP could be used to simplify and accelerate HM fabrication. Furthermore, since deposition selectivity is also achieved through AR shading, it can be adopted to process materials other than C-masks and SiO_2 etching targets, as well.

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