Plasma Science and Technology Division
Room A106 - Session PS-TuM

Plasma Processing for Advanced Logic Device Fabrications

Moderators: John Arnold, IBM Research Division, Albany, NY, **Tetsuya Tatsumi**, Sony Semiconductor Solutions Corporation

8:00am **PS-TuM-1 Chemical Role of a Small Amount of Cl--₂ in O_2/Cl_2 Plasma for Ru Etching Reaction***, **Masaya Imai**, M. Matsui, R. Sugano,* Hitachi, Ltd., Japan*; T. Shiota, K. Takasaki,* Hitachi High Technologies, Japan*; Y. Ishii,* Hitachi High Technologies America Inc.*; M. Miura, K. Kuwahara,* Hitachi High Technologies, Japan

Ruthenium (Ru) is an attractive candidate as an interconnect metal for future semiconductor devices which can replace conventional copper (Cu). This is because the Ru interconnect below 20-nm-pitch shows a lower resistivity and a higher electromigration reliability than Cu one. Especially, direct patterning of Ru is expected to maximize those advantages. In the patterning process of Ru, the dry etching with oxygen-based plasma is applied because Ru tetraoxides (RuO_4) are volatile. Several reports using reactive ion etching (RIE) showed that the etch rate of Ru is the highest using a O_2/Cl_2 plasma with a 10–20% amount of Cl_2, while it is lower when using pure O_2. The etch rate is also lower when Cl-rich plasma is applied due to the formation of non-volatile Ru chlorides. However, it has not been clarified why a small amount of Cl_2 in the plasma promotes the etching reaction and why the Ru is not etched by pure O_2 plasma.

In this work, the etching reaction mechanism on the Ru surface using a O_2/Cl_2 plasma was investigated by experiments and simulations. Our electron cyclotron resonance (ECR) etcher is unique in that only radicals in the plasma reach the wafer by removing reactive ions using an ion shield plate. Applying this etching technique, we found that Ru can be etched by only radicals in O_2/Cl_2 plasma and that the etch rate was the highest with a ~10% amount of Cl_2. Therefore, a small amount of Cl-based radicals in the plasma explicitly contributes to the chemical reactions to form volatile Ru products, such as RuO_4 and $RuCl_xO_y$.

Using density functional theory (DFT) simulation, we modeled the atomic configuration on Ru surfaces where O and Cl radicals react. In our unit cell, there are nine chemisorption sites for O and Cl. We prepared three surface models where (1) all nine chemisorption sites were covered by O, (2) one chemisorption site was covered by Cl atom and the other eight were covered by O atoms, and (3) two adjacent chemisorption sites were covered by two Cl atoms and the other seven were covered by O atoms. Subsequently, we assumed that the volatile Ru products are formed by the oxidation reactions of the surface Ru atoms. Using nudged elastic band (NEB) method, we calculated the activation energies to desorb the volatile Ru products depending on the surface coverage of chemisorbed O and Cl. Comparing the activation energy among the three surface models, we revealed that it decreases as the number of chemisorbed Cl increases. We concluded that a small amount of Cl_2 in the O_2/Cl_2 plasma contributes to decreasing the activation energy to form volatile Ru products on the surface, resulting in increasing the etching rate of Ru.

8:20am **PS-TuM-2 Coupling of Deposition and Etching to Achieve Selective Removal of TaN with Respect to Ultra Low-*k* Dielectric***, **Ivo Otto IV**,* SUNY Polytechnic Institute*; C. Vallée,* SUNY Polytechnic Institute, France

The transition from silicon oxide and aluminum in the back-end-of-the-line (BEOL) to ultra low-*k* dielectric (ULK) and copper improved RC delay, but came with key challenges, one of which was copper diffusion into the ULK. Diffusion barriers are required in current integration schemes in order to mitigate copper diffusion, and TaN is a key diffusion barrier candidate because of strong dielectric adhesion and low in-plane resistivity properties at sub-5 nm thicknesses. Creation of the BEOL interconnect superstructure is completed in a cyclical fashion, requiring the repeated selective removal of not only copper, but the TaN diffusion barrier selective to the ULK. The TaN diffusion barrier directly contacts the ULK, making selectivity to the ULK of primary importance for this step. ULK films are susceptible to radical-dominated, fluorine-based etching because of the weak bond strength of methyl groups, high porosity allowing high accessibility, and high volatility of SiF_2, SiF_4, and CF_x etch byproducts. The inherent fluorine-based etching pathways make selective fluorine etching of TaN with respect to ULK challenging but may be overcome by coupling of etching and deposition regimes. Plasma-assisted chemical vapor deposition of Si, SiO_2, and SiOF films have been previously explored with Si-containing precursors such as SiF_4 and $SiCl_4$, with additives such as O_2 and H_2 used to manipulate deposited film stoichiometry and film properties. In this work, we explore the use of aforementioned Si-precursors and additives injected directly into an inductively-coupled discharge to perform a protective deposition on the ULK film, while etching the TaN film. The discharge is maintained without applied biasing and at a pressure to remove ion bombardment and allow deposition and etching mechanisms to be radical dominated and isotropic in nature. The focus is mainly the modulation of SiF_4 regimes by exploration of the addition of O_2 or H_2 with modulation of electrostatic chuck temperature, plasma discharge power, and injected species concentration. Ex-situ spectroscopic ellipsometry is utilized with support of scanning electron microscopic imaging to characterize film thickness changes. In-situ optical emission spectroscopy is utilized to better understand the plasma discharge species concentrations and the relevance to observed film thickness modulation. Ex-situ X-ray photoelectron spectroscopy is additionally used to probe the sample surface environment to characterize surface film properties. Though this investigation the possibility of selective deposition on ULK while simultaneously etching TaN is found to be possible by modulation of the aforementioned regimes.

8:40am **PS-TuM-3 Using Metal-Based Photoresists and Hard Masks for Patterning Process Window Expansion***, **Joe Lee**, Y. Mignot, S. Sieg, C. Penny, K. Motoyama, K. Petrillo,* IBM Research Division, Albany, NY*; E. Liu, S. Thibaut, C. Cole,* Tokyo Electron Ltd.

Scaling of critical dimensions calls for greater control of processing conditions for smaller nodes. As such, materials with greater etch selectivity are required to successfully pattern with a healthy process window. Plasma etch tuning can only stretch so far as current schemes face an increasingly heavy burden of walking a tightrope to balance the conservation of photoresist or masking layers while ensuring good clearance of underlying materials. The introduction of metal-containing masking layers, including metalorgano resists (MOR) and metal hard masks, greatly alleviate the burden of traditional soft-mask layers that are more easily deformed during etching. We show schemes that implement its usage, yielding a vast array of benefits, such as reduction of defectivity and roughness in lines, increased flexibility of processing conditions, and a larger process window for structures with aggressive aspect ratios that would otherwise be extremely challenging to produce. Such metal-containing masking layers provide a great benefit to the integrity of multipatterned mandrel structures where pitch doubling is required. As dimensions grow more aggressive, any techniques to alleviate patterning challenges and reduce cycles of learning would be greatly welcome.

9:00am **PS-TuM-4 Understanding Etching of Nanoscale Structures Using Molecular Dynamics and Plasma Modeling***, **Xingyi Shi**, S. Rauf, J. Wang, J. Kenney,* Applied Materials*; J. Booth,* LPP-CNRS, France*; Y. Azamoum,* Helmholtz Institute Jena, Germany*; M. Foucher,* LPP-CNRS, France

Pulsed plasmas are widely used in the semiconductor industry because of the flexibility they offer in controlling etch and deposition processes. Pulsed plasmas allow one to modulate the flux of energetic ions and neutral radicals to the substrate on a millisecond or faster timescale. As the semiconductor industry transitions to sub-5 nm technology nodes, pulsed plasma processes are becoming exceedingly complex due to the need to control surface processes with atomic precision. In this paper, we examine a pulsed chlorine plasma and its interaction with silicon substrates though a combination of fluid plasma simulations, molecular dynamics modeling, and feature scale flux calculations. First, we model the inductively coupled Cl_2 plasma for a range of pressures and powers. The plasma modeling results are compared to experimental measurements of electron density (by microwave hairpin resonator probe) and Cl density (by TALIF with absolute calibration [1]). The validated plasma model is also used to compute the ion angular and energy distribution with pulsed DC bias at low frequency.

From the plasma simulations, we obtain the fluxes and ion angular and energy distributions for the dominant etch species at different pulsing conditions. Cl radicals and Cl_2^+ ions are the primary species in inductive coupled Cl_2 plasma. We then compute the flux distributions for these species inside trench shaped features with aspect ratios ranging from 1 to 100. Due to the directionality of the charged ion species, the ion flux at the bottom of the feature is nearly the same as that at the top of the feature. In contrast, with increasing aspect ratio, fewer radicals can reach the bottom of the feature, resulting in a decrease in the radical to ion flux ratio.

The impact of the change in the flux ratio is examined through molecular dynamics simulations. Based on the flux ratios from the previous analysis, different combinations of chlorine radicals and Cl_2^+ ions at 100eV bombard

a bare silicon surface. We observe that the silicon etch yield increases at low Cl/Cl_2^+ flux ratio and plateaus at large flux ratios.

[1] Booth, J. P., Azamoum, Y., Sirse, N., & Chabert, P. (2012). Absolute atomic chlorine densities in a Cl2 inductively coupled plasma determined by two-photon laser-induced fluorescence with a new calibration method. *Journal of Physics D: Applied Physics*, 45(19), 195201.

9:20am **PS-TuM-5 Technology Options to Enable Logic Scaling in Advanced BEOL from Patterning to Metal Interconnect Formation***, **Eric Liu**, A. Ko, N. Joy, S. Rogalskyj, S. Grzeskowiak, A. Krawicz, K. Kanzo, L. Huli, P. Biolsi,* TEL Technology Center, America, LLC **INVITED**

The Back-End-Of-Line (BEOL) process is a crucial step in manufacturing advanced semiconductor logic devices. Recent advancements in EUV lithography, self-aligned multi-patterning, and ruthenium subtractive interconnect formation have led to the developing of more powerful and efficient devices.

EUV lithography employs shorter wavelengths of light to create finer and more complex circuit patterns, enabling the fabrication of smaller interconnects and vias with reduced edge-placement-error and line roughness. This technology has significantly contributed to extending the roadmap of device scaling and reducing the process/design complexity. Self-aligned multi-patterning is another key technique that uses several steps to create a single layer of patterned material with multiple, smaller patterns. This approach enables the self-alignment technique to fabricate more precise and complex circuits with manageable pattern placement and overlay accuracy. Finally, ruthenium subtractive interconnect formation is a novel process that has created interconnects with lower resistance, improved reliability, and overcome the fundamental challenge of RC delay from the conventional damascene approach with copper.

In this presentation, we examine several technology options and innovations to realize the formation of metal interconnects in a critical layer. These innovations include:

1. Advancements in EUV lithography and self-aligned multi-patterning.
2. Patterning consideration between CAR (chemically amplified resist) and MOR (metalorganic resist).
3. Plasma etch interaction to the interconnect material and pattern fidelity.

Meeting the physical and electrical requirements is essential to continuous scaling in advanced BEOL.

11:00am **PS-TuM-10 Direct Ru Etching Mechanism for Advanced Interconnect***, **Miyako Matsui**,* Hitachi, Ltd., Japan*; Y. Ishii, L. Kovatch, K. Maier,* Hitachi High Tech America Inc.*; M. Miura, K. Kuwahara,* Hitachi High Tech, Japan

Logic devices are being continuously scaled by fabricating three-dimensional structures. The recent scaling has been achieved by both pitch scaling and various boosting technologies, such as design technology co-optimization. With the device scaling, alternative metal integrations are also required that enable shrinkage of metal pitch at the back end of the line. Ru is a candidate for interconnect material with metal pitches of 20 nm and beyond, because the Ru interconnect is expected to have lower effective resistance than the Cu interconnect at such small pitches. In addition, Ru is expected to be etched directly, which leads to new scaling boosters, such as semi-damascene patterning. To realize such patterning technology, Ru patterns need to be vertically etched with high selectivity for hard masks. In addition, roughness or other damage should be suppressed to reduce interconnect resistance. In this study, we investigated a Ru etching mechanism using a microwave-ECR etching system. The composition of the etched surface was analyzed by using X-ray photoelectron spectroscopy (XPS), and roughness was measured by using atomic force spectroscopy (AFM).

Ru was etched with high selectivity using Cl_2/O_2 plasma in regard to various materials used for hard masks, which were TiN, Poly-Si, SiO_2, and Si_3N_4. The Ru etch rate was the highest when 20% of Cl_2 gas was added to the Cl_2/O_2 plasma. In that condition, Ru surface was etched by forming volatile RuO_4 or $RuCl_xO_y$, and a smooth surface was obtained after etching. However, when using O_2-rich plasma, nonvolatile RuO_2 was formed, which seems to cause the surface roughness. When using Cl_2-rich plasma, formation of nonvolatile $RuCl_x$ reduced the Ru etch rate and generated the surface roughness by forming micro masks.

We also evaluated a line-and-space Ru pattern with 32-nm-pitch using Cl_2/O_2-based plasma. Selectivity over the Si_3N_4 mask and the Ru sidewall roughness were changed by ion flux, which was adjusted by the duty cycle of wafer bias power using Cl_2/O_2 plasma. When the wafer bias was applied continuously, the Si_3N_4 hard mask widened due to the Si containing by-product. When the ion flux was decreased by reducing a duty cycle of wafer bias, the Ru pattern was vertically etched, but larger sidewall roughness was formed. The roughness was thought to be formed because the sidewalls, on which non-volatile RuO_x and $RuCl_y$ were formed, were etched by O and Cl radicals during the off period of the wafer bias power. We suggested adding a passivation gas to the Cl_2/O_2 plasma to reduce sidewall roughness. Sidewall roughness was thought to be reduced because the sidewalls were uniformly protected from the etching.

11:20am **PS-TuM-11 Study and Characterization of Thick Beol Dual Damascene Self- Aligned via Indenting Etch for Bcd Smart Power Technology Node***, **Pietro Petruzza**,* ST Microelectronics, Italy

Development and characterization of plasma etching processes of manufacturing dielectric self-aligned dual damascene etch for thick Cu BEOL metallization. DD process is carried out by a new reactive ion etching (RIE) employing with RF capacitive-coupled parallel plate plasma (CCP) for BCD smart power 110 nm technology node. The method is accomplished by providing a first inter-level dielectric, SiN via etch (indenting), depositing a second inter-level dielectric layer on the silicon nitride layer; finally selective patterning of line on second inter-level dielectric layer and vias on first inter-level dielectric. These applications require fine patterning of dielectric films by reactive ion etching (RIE) process. Precise control of critical dimensions (CD), etch profile and higher aspect ratio of DD etch are essential factors. Via first DD self-aligned approach increasingly require etching the trench without a stop layer. This place exacting demands on etch uniformity, etch front control and sidewall profile, angle control, micro-trenching effect and it becomes difficult to satisfy high selectivity with minimal small micro-loading at same time. The impact of these issues is crucial when the aspect ratio is very high and on the device are present several patterning structures, typical of smart power technology: ISO and dense with different wide and space. The results show that the loading can be improved and kept at same level when the recess depth increasing.We investigated the DD etching in terms of etching process parameters such as pressure, gas: polymerization gas /O2 mixed, C to F ratio, gas flux directionality, increasing the upper frequency, power. At the same time also the multilayer stack of DD was modulated to meet the requirements of dry etching in terms of robustness and reliability. Using the obtained result, we have provided an etching process with suitable process parameters in order to realize high performance and low-cost semiconductor devices.

11:40am **PS-TuM-12 Process Development of Selective ICP Etching of Si_3N_4 over SiO_2 and of SiO_2 over Si_3N_4 to Produce Dense Arrays of 50 nm Patterns***, **Andréa Fassion**, A. Sarrazin, T. Chevolleau,* Univ. Grenoble Alpes, CEA, Leti, France

The transition of silicon spin qubits from 1D (Dimension) devices to 2D ones demands to produce new architectures and develop dedicated patterning processes **[1]**. To produce the 2D silicon spin qubits devices developed at CEA-Leti, dense and low dimension arrays of patterns are required. 50 nm-wide square-based holes have to be obtained on a thin layer of Silicon On Insulator (SOI) using a crossbar Litho-Etch-Litho-Etch (LELE) scheme. It combines two thin (i.e. 10-40 nm thick) hard mask layers consisting of SiO_2 on Si_3N_4. This patterning scheme requires the anisotropic etching of Si_3N_4 with a high selectivity over SiO_2 and vice-versa.

A previous study showed that a CH_3F/O_2 based plasma allows the etching of Si_3N_4 with a high selectivity over SiO_2 **[2]**. Regarding the selective etching of SiO_2 over Si_3N_4, a recent work presents a process using a BCl_3/Ar based plasma reaching a selectivity of about 4:1 **[3]**. The work presented here aims to further characterize the selectivity mechanisms of both CH_3F/O_2 and BCl_3/Ar based processes.

Etching is performed in an industrial ICP (Inductively Coupled Plasma) reactor. The etching mechanisms are discussed in terms of plasma-surface interactions. These interactions are characterised using in-situ Optical Emission Spectroscopy (OES) and interferometry, ex-situ Spectroscopic Ellipsometry (SE), X-Ray Reflectometry (XRR), Atomic Force Microscope (AFM) and quasi in-situ X-Ray Photoelectron Spectrometry (XPS).

Our study shows that CH_3F/O_2 based processes reach an etching selectivity higher than 15:1 and that it strongly relies on the use of F-poor fluorinated gas, high amount of O_2 and high-pressure conditions (figures enclosed). Our

work also reveals that BCl_3/Ar based processes selectivity relies on both bias voltage and the operating pressure (figures enclosed). It also shows that BCl_3/Ar based process enable a SiO_2 etching ranging from 2 to 15 nm.min^{-1} with a selectivity over Si_3N_4 of 7:1 and 3:1, respectively.

According to these selective and low etch rate processes, alternative integration strategies are proposed and applications to patterns will be presented.

References

[1] M. Vinet, Nature nanotechnology **16**, 1296 (2021).

[2] H. Ohtake et al. Jpn. J. Appl. Phys. **55**, 086502 (2016).

[3] M. Matsui, K.Kuwahara Jpn. J. Appl. Phys. **57,** 06JB01 (2018).

12:00pm **PS-TuM-13 Plasma etch study of $Nb_xTi_{(1-x)}N$ metal lines for Superconducting Digital Logic***, **Yann Canvel,** L. Souriau, V. Renaud, A. Pokhrel, A. Gupta, M. Kim, J. Soulie, S. Sarkar,* IMEC, Belgium*; A. Herr, Q. Herr,* IMEC*; F. Lazzarino, Z. Tokei,* IMEC, Belgium

In the development of next-generation logic devices, an attractive complement to CMOS technology would be to leverage the superconducting technology which operates at a low temperature. Superconducting Digital Logic (SDL) devices are attractive as they are inherently faster and have much less power dissipation than their CMOS counterpart. Although SDL devices have existed for decades now, there have been fundamental challenges to scale down its main components and related interconnects. To provide groundwork for exploring SDL device integration, and a possible hybrid integration of SDL/CMOS circuits, one of the key patterning challenges is the backend fabrication of superconducting metal lines using direct metal etch (DME) approach at relatively small CD/pitch dimension.

In this communication, an in-depth plasma etch investigation is reported to demonstrate the patterning of $Nb_xTi_{(1-x)}N$ wires. Using the Reactive Ion Etching (RIE) technique, the study has firstly consisted of screening the plasma chemistry and the tool-related parameters. It has provided some solid learnings to roll out a process optimization, leading to the successful fabrication of $Nb_xTi_{(1-x)}N$ metal lines at CD of 50 nm and pitch of 200 nm. Finally, some electrical measurements at room and cryogenic temperatures will complete the investigation validating the fabrication of the smallest superconducting interconnects ever produced.

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