Electronic Materials and Photonics Division
Room 304 - Session EM2-FrM

Advanced Devices & Fabrication Methods

Moderators: Parag Banerjee, University of Central Florida, **Bryan Wiggins**, Intel Corporation

10:40am **EM2-FrM-8 Two-Dimensional Steep-Slope Transistors Using Graphene Cold Sources**, *M. Liu, H. Jaiswal, S. Shahi, S. Wei, Y. Fu, A. Chakravarty, A. Cabanillas, A. Ahmed, F. Yao, **Huamin Li,*** University at Buffalo

Two-dimensional (2D) steep-slope field-effect transistors (FETs) with low energy consumption have been considered to have great potential to continue the future exponential growth of semiconductor electronic devices. The performance of conventional 2D transistors is limited by "Boltzmann tyranny" which generates a relatively long thermal tail in energy distribution and limits the subthreshold swing (SS) at 60 mV/decade at room temperature. To break the limit of 60 mV/decade SS, tunneling FETs (TFETs) and negative capacitance FETs (NCFETs) have been proposed, yet they suffer a variety of challenges and issues. Here we investigate an emerging concept of the steep-slope transistors known as cold-source FETs (CSFETs) or Dirac-source FETs (DSFETs) where graphene (Gr) serves as the Dirac source to provide the cold electrons with a localized electron density distribution and a short thermal tail at room temperature, as shown in Fig. 1. For the CSFET with monolayer MoS2 as the 2D channel, the transport factor can be reduced due to the localized electron density distribution and a shorter thermal tail, giving rise to a minimum SS of 29 mV/decade at room temperature, an excellent on/off ratio (~107), and a record high sub-60-mV/decade current density (~4 µA/µm) which are comparable to current steep-slope technologies, as shown in Fig. 2. Similarly, the CSFET with a multilayer WSe2 channel also shows a sub-60-mV/decade SS, as shown in Fig. 3. The 2D MoS2 and WSe2 CSFETs in this work are benchmarked with the 14 nm Si-based FinFET CMOS technology, as shown in Fig. 4 (a). The sub-60-mV/decade SS as a function of drain current (JD) was compared with other steep-slope transistors, including TFETs, NCFETs, and one-dimensional (1D) CSFETs based on a variety of channel materials, as shown in Fig. 4(b). Our work demonstrated the 2D CSFETs as a steep-slope transistor concept for energy-efficient beyond-CMOS technology.

11:00am **EM2-FrM-9 High Performance, RF Interposer Fabrication on Glass with 3 Metal Layers and Embedded TGVs**, *S. Herrera, A. Ruyack, S. Lepkowski, M. Hirabayashi, M. Powner, C. Nordquist, **Matthew Jordan,*** Sandia National Laboratories

We will show the fabrication of a 3-metal layer, low-k dielectric, interposer on glass capable of supporting RF and optoelectronic microsystems. Multi-chip modules (MCMs) allow for the combination of several disparate technologies, like wide bandgap MMICs (monolithic microwave integrated circuits) and CMOS mixed signal electronics, in one package. However, wirebond compatible MCMs suffer from long interconnect lengths as well as require many of the passive RF circuit components to be either incorporated on-chip (a loss of active space) or on the printed circuit board (increasing manufacturing complexity). In fact, much of the footprint of a typical RF chip is devoted to passive components such as decoupling capacitors and impedance matching networks. Disaggregating RF circuit components from transistor technologies through repeatable methods of interconnecting RF chips will reduce on-chip real estate leading to decreased cost. Removing components from the circuit board decreases the manufacturing complexity, as well as size, weight, and power. Therefore, an intermediate interposer that both improves upon MCM performance and reduces cost is an attractive solution.

The interposer approach discussed in this presentation utilizes a flip-chip method to electrically connect die, resulting in repeatable connections between the interposer and the die. This differentiates the approach from similar RF interposer methods like the HRL MECAMIC process in which die are embedded in the interposer[Herrault2020]. Integrated passive devices on the interposer include metal-insulator-metal capacitors, resistors, and inductors which further simplify RF integrated circuit chip design.

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11:20am **EM2-FrM-10 Single Step Fabrication Process of Alignment Markers for Direct-Write Electron Beam Lithography in Metal-Organic Negative Tone Resist**, ***Guy DeRose,*** California Institute of Technology

Alignment markers, also referred to as fiducial marks, are commonly made by a process called liftoff. In the liftoff process, a bilayer electron beam resist, such as polymethyl methacrylate (PMMA), is spun and baked onto the substrate, then written by the electron beam pattern generator. Following the development of the resist, a metallization step, typically electron beam evaporation, takes place, followed by soaking the coated substrate in a solvent such as N-Methylpyrrolidone (NMP) during which the metal that is not stuck to the substrate "lifts off" and leaves behind the alignment markers of interest. While a standard process, there are many steps involved, and it is possible that the evaporation process might not be compatible with subsequent steps in the fabrication.

Previously we have demonstrated a negative tone resist that is comprised of a metal-organic material [1]. Using electron beam lithography, we have shown that it can produce high fidelity patterns of 15 nm half pitch. To build upon this work, we demonstrate the fabrication of the alignment markers by directly writing them into this resist in a single process step. Due to the fact that the resist contains chromium metal it was hypothesized that the metal content may be detected by the secondary electron detector (SED) has the metal would produce higher contrast. It can be seen from X-ray photoelectron spectra (XPS) of Figure 2 that the resist has reduced into a metallic oxide material to form CrO_x after it has been exposed by the electron beam; this means that the resist material is no longer soluble in the developing solvent, hence a pattern can be formed. The material can also be used as alignment markers because the density contrast between the silicon and the CrO_x material is dramatically increased by a factor of ~2.25 and this inherently increases the effective atomic number contrast which allows them to be detected by the SED, which can be seen by the Monte Carlo simulations of Figure 3. Figure 4 shows the results of writing an array of 20 um square alignment marks, which are commonly used for multi-layer electron beam lithography.

It can be seen by the SED that the pattern shows high pattern quality. We have demonstrated this at 20 KeV, however, we will present the results of using these patterns as alignment markers for direct-write electron beam lithography at 30 KeV and 100 KeV, along with detailed Monte Carlo simulations that describe the interaction between the incident electron beam and the resist/substrate combination.

11:40am **EM2-FrM-11 Non-Destructive Metrology Techniques for Characterizing a-C Hard Mask Films in 3D NAND Structures**, *P. Mukundhan, **G. Andrew Antonelli,*** Onto Innovation

Growth in 3D NAND is driven by data-intensive applications that have changed the paradigm for manufacturing to achieve vertical scaling. One of the key steps in the process is the use of hardmask deposition to etch deep, high-aspect ratio features that conventional photoresist cannot withstand. Amorphous carbon (a-C)-based hard masks, grown using plasma-enhanced chemical vapor deposition (PECVD) have been adopted in high volume manufacturing.

Depending on the process condition, these films exhibit a wide range of hardness, electrical resistivity, optical transparency, and chemical inertness. The information needed during design of the material includes thickness uniformity, characterization of optical constants, density, elastic modulus, and bonding structure. The sp^3-to-sp^2 hybridization ratio and the H content determine the thermomechanical properties of the films. Given the complex nature of an a-C system, no single metrology technique provides all the relevant information needed for process tuning.

In this paper, we present results from two non-destructive techniques: picosecond ultrasonics (PULSE™) and FTIR for the qualification of next generation of advanced hard mask materials. A design-of-experiments (DOE) skew (~3µm a-C thickness target) covering different deposition temperature, pressure and time were generated. With the transition of a-C to thicker and more graphitic (opaque) films, the PULSE™ technique is uniquely qualified for measuring thickness and elastic modulus of these films. Results from the systematic study of different types of films demonstrated sensitivity to process variation and excellent correlation to cross-section microscopy. A second set of a-C films in the 0.2 µm -2µm thickness range was generated to test sensitivity to different processes and provide information regarding the bonding characteristics. Studies have shown the correlation between structural characteristics and the etching characteristics which is primarily determined by the sp3/sp2 ratio. Wafer maps have been collected using an Element™ 300mm automated FTIR. We observed that the absorbances for the sp^2 C=C and the sp^3 C-H_x stretching

bonds were significantly different and could be used to discriminate the processes. Furthermore, the sp^2/sp^3 ratio was successfully calculated for all samples. Current efforts are focused on finding correlation between the two metrology techniques and their application in etch process optimization for high volume manufacturing.

Author Index

Bold page numbers indicate presenter

— A —
Ahmed, A.: EM2-FrM-8, 1
Antonelli, G.: EM2-FrM-11, **1**
— C —
Cabanillas, A.: EM2-FrM-8, 1
Chakravarty, A.: EM2-FrM-8, 1
— D —
DeRose, G.: EM2-FrM-10, **1**
— F —
Fu, Y.: EM2-FrM-8, 1
— H —
Herrera, S.: EM2-FrM-9, 1
Hirabayashi, M.: EM2-FrM-9, 1
— J —
Jaiswal, H.: EM2-FrM-8, 1
Jordan, M.: EM2-FrM-9, **1**
— L —
Lepkowski, S.: EM2-FrM-9, 1
Li, H.: EM2-FrM-8, **1**
Liu, M.: EM2-FrM-8, 1
— M —
Mukundhan, P.: EM2-FrM-11, 1
— N —
Nordquist, C.: EM2-FrM-9, 1
— P —
Powner, M.: EM2-FrM-9, 1
— R —
Ruyack, A.: EM2-FrM-9, 1
— S —
Shahi, S.: EM2-FrM-8, 1
— W —
Wei, S.: EM2-FrM-8, 1
— Y —
Yao, F.: EM2-FrM-8, 1