Nanoscale Science and Technology Division
Room 304 - Session NS1+QS-MoM

Fabrication, Testing and Metrology of Quantum Devices and Systems

Moderator: Wonhee Ko, Oak Ridge Natinal Laboratory

8:20am **NS1+QS-MoM-1 Single Electrons on Solid Neon: A New Solid-State Qubit Platform with Ultralong Coherence***, **Xianjing Zhou**,* Pritzker School of Molecular Engineering, University of Chicago **INVITED**

Progress towards the realization of quantum computers requires persistent advances in their constituent building blocks—qubits. Novel qubit platforms that simultaneously embody long coherence, fast operation and large scalability offer compelling advantages in the construction of quantum computers and many other quantum information systems. Electrons, ubiquitous elementary particles of non-zero charge, spin and mass, have commonly been perceived as paradigmatic local quantum information carriers. Despite superior controllability and configurability, their practical performance as qubits through either motional or spin states depends critically on their material environment. In this talk, I will present our experimental realization of a new qubit platform based on isolated single electrons trapped on an ultraclean solid neon surface in vacuum. By integrating an electron trap in a circuit quantum electrodynamics architecture, we achieve strong coupling between the motional states of a single electron and a single microwave photon in an on-chip superconducting resonator [1]. Qubit gate operations and dispersive readout are successfully implemented. Our latest measurements show that both the relaxation time T_1 and coherence time T_2 have reached 0.100-millisecond scale [2]. The observed single-shot readout fidelity, without using a quantum-limited amplifier, is already 94.4%. Simultaneous strong coupling of two qubits with the microwave resonator is also demonstrated, as a first step toward two-qubit entangling gates for universal quantum computing. These results manifest that the electron-on-solid-neon (eNe) charge qubits have outperformed all the existing charge qubits to date and rivaled the state-of-the-art superconducting transmon qubits.

[1] X. Zhou … and D. Jin, "Single electrons on solid neon as a solid-state qubit platform", Nature 605, 46–50 (2022).

[2] X. Zhou … and D. Jin, "Electron charge qubits on solid neon with 0.1 millisecond coherence time", manuscript submitted (2022).

9:00am **NS1+QS-MoM-3 Ultra-thin TaN Damascene Nanowire Structures on 300 mm Si Wafers for Quantum Applications***, **Ekta Bhatia**, S. Kar, S. Olson, T. Vo, S. Schujman, J. Nalaskowski,* NY CREATES*; H. Frost,* SUNY Polytechnic Institute, Albany*; J. Mucci, B. Martinick, I. Wells, T. Murray, C. Johnson, V. Kaushik, S. Papa Rao,* NY CREATES

Tantalum nitride (TaN) is a material which has been used as a copper diffusion barrier in integrated circuits, along with many other applications ranging from corrosion-resistant coatings to superconducting quantum devices. Superconducting nanowire single photon detectors (SNSPDs) are critical for applications in photonic quantum computing, single-flux quantum logic circuits for qubit readout, and neuromorphic computing. TaN SNSPDs have been shown to extend the detection bandwidth to longer wavelengths, along with higher detection efficiency, enabling new applications in cosmology when fabricated into large scale arrays. TaN devices at 300 mm wafer scale can leverage the advances made by the semiconductor industry in process control, improving yield, pattern fidelity and wafer-to-wafer predictability of performance. Hence, the development of this process technology will enable large scale SNSPD arrays, and will also be useful for superconducting circuits for quantum applications.

Detailed studies of the influence of nitrogen content on the superconducting characteristics of TaN thin films are not widely available in the literature, particularly at 300 mm wafer scale. We report the development of ultra-thin reactive sputtered TaN films prepared with different Ta to N ratios on 300 mm scale. We fabricated damascene structures of TaN nanowires with widths varying from 100 to 3000 nm and thickness varying from 5 to 35 nm using 193 nm optical lithography and advanced chemical mechanical planarization.

We confirmed a sigmoidal dependence of TaN sheet resistance on Ta to N ratio, and a decrease in crystallite size (extracted from XRD measurements). The superconductor to insulator transition as a function of Ta to N ratio is reported. We will also discuss the influence of encapsulation of the superconducting wires with metallic TaN and copper. Cu encapsulation can improve contact resistance during measurement, and has implications for thermal conduction along the length of the superconducting nanowire. In contrast, adding an intervening layer of highly disordered metallic TaN between the superconducting TaN and Cu ensures minimal leakage of Cooper-pairs at TaN/Cu interface. We will report the variation of T_c and J_c of TaN nanowires as a function of film thickness, material characteristics, Ta to N ratio and encapsulation.The potential of ultra-thin TaN films at 300 mm scale will be discussed in the context of applications such as on-chip integration for readout of superconducting qubits, in quantum phase slip studies, and large focal-plane detector arrays for cosmology.

9:20am **NS1+QS-MoM-4 Direct Integration of Atomic Precision Devices into a MOS-Compatible Process***, **Jeffrey Ivie**, D. Campbell, A. Leenheer, C. Halsey, E. Anderson, S. Schmucker, D. Scrymgeour, X. Gao, W. Lepkowski, T. Lu, L. Tracy, S. Misra,* Sandia National Laboratories

Atomic precision advanced manufacturing (APAM) of electrical devices, fabricated using hydrogen depassivation lithography in a scanning tunneling microscope, offers a way to explore device physics with the ultimate degree of control. Almost all previous work has focused on exploring applications in quantum physics, particularly with a focus on qubits, using devices operating at cryogenic temperatures. While APAM may benefit applications in microelectronics, such as the strong doping of contacts in scaled transistors, the high temperature surface preparation of APAM generally makes it incompatible with modern metal-oxide semiconductor (MOS) process flows. To leverage significant past investments in CMOS manufacturing and enable a wider application space for APAM devices, demonstration of direct integration of APAM into existing MOS process flows is required.

To enable direct integration of APAM devices, we have established a natural insertion point for APAM processing between Front-end-of-line (FEOL) and Back-end-of-line (BEOL) steps on Sandia's 0.35-micron CMOS node. The insertion point allows for readily accessed device Si through gentle sputtering and thermal annealing, which has a sufficiently crystalline surface critical for APAM delta doping. Integration of the moderate temperature APAM processing step (<600 °C) between high temperature FEOL processing (1000 °C) and before low temperature BEOL processing (<400 °C) maintains the electrical characteristics of both the inserted APAM delta-doped material and the discrete transistors and integrated circuit components from FEOL. Furthermore, accelerated lifetime measurements of APAM wires demonstrate that patterned APAM material is more robust than standard metal features in modern CMOS devices. Establishing the capability of direct integration of APAM into a CMOS process flow opens the door to enhance CMOS transistors with APAM-based processing along with providing wider manufacturing interest. Similarly, implementation of novel APAM-based devices alongside CMOS circuits is a significant discovery platform for microelectronics, neuromorphic computing hardware, or hybrid quantum applications.

This work was supported by the Laboratory Directed Research and Development Program at Sandia National Laboratories and was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. DOE, Office of Basic Energy Sciences user facility. SNL is managed and operated by NTESS under DOE NNSA contract DE-NA0003525. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government.

9:40am **NS1+QS-MoM-5 Low Thermal Budget PMOS in Low Temperature Epitaxial Silicon***, **Christopher Allemang**, D. Campbell, J. Ivie, T. Lu, S. Misra,* Sandia National Laboratories

Atomic precision advanced manufacturing (APAM) enables deposition of dopants in silicon (Si) with atomic precision and has been exploited to make donor-based qubits. However, understanding the electrical effects of the process tradeoffs in burying the dopants under an epitaxial Si capping layer grown at low temperatures has remained a challenge, both for qubits and for other microelectronics applications. This cap layer can be deposited at the lowest temperatures to limit the diffusion of dopants, or at modest temperatures to limit the density of point defects. Here, to evaluate the electrical quality of the Si cap, we explore using APAM materials and compatible processes for other microelectronic devices, namely p-type metal-oxide-semiconductor (PMOS) field-effect transistors.

The Si cap is unintentionally doped with aluminum during the growth process leading to a p-type material. To employ this p-type material for PMOS, we must have ohmic contacts and a way to gate the channel.

Typical processes used for contacting and gating the channel, e.g. implants and thermal oxide, cannot be used here because they are high temperature processes. To maintain an APAM compatible thermal budget, we have developed ohmic contacts to the cap layer using platinum silicide formed at 400ºC and an atomic layer deposition Al_2O_3 gate oxide grown at 250ºC. These temperatures are also within the back-end-of-line thermal budget for Si CMOS, implying this process could be used to integrate an additional device layer on an existing chip.

The silicide contacts are qualified by fabricating Schottky diodes on n-type material and analyzing their current-voltage (*IV*) characteristics, while the gate oxide is qualified by measuring the capacitance-voltage characteristics of MOS capacitors. Further, these processes are combined to demonstrate PMOS transistor behavior in APAM material for the first time. The electrical transport in the cap layer is then qualified using *IV* measurements. While these results represent the initial qualification of electrical transport in the cap layer, further studies and analysis may reveal impacts to APAM quantum devices.

This work was partially funded by the Advanced Manufacturing Office project Big Energy Efficient Transistors, supported by the Laboratory Directed Research and Development Program at Sandia National Laboratories, and performed, in part, at the Center for Integrated Nanotechnologies, a U.S. DOE, Office of Basic Energy Sciences user facility. SNL is managed and operated by NTESS under DOE NNSA contract DE-NA0003525. The views expressed here do not necessarily represent the views of the DOE or the U.S. Government.

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