On Demand available October 25-November 30, 2021

Manufacturing Science and Technology Group
Room On Demand - Session MS-Contributed On Demand

Manufacturing Science and Technology Contributed On Demand Session

MS-Contributed On Demand-1 Machine Learning and Simulation Assistant Technology to Facilitate 3d Memory Analysis of Cross Section Sem Images*, M. Bryan, J. Foucher,* ***Julien Baderot****,* POLLEN Metrology, France

We present a method for fast, enhanced cross-section SEM metrology of 3D memory channels through simulation and machine learning. Using simple geometric models of the channel structure and certain assumptions on the behaviour of the electron beam we demonstrate that our method provides increased robustness to acquisition errors and gives more physically meaningful measurements of 3D memory when compared to traditional image processing-based techniques. We show also how this technique can be integrated into the Process Engineer workflow during semiconductor research and development, providing actionable results faster and reducing overall time-to-production

MS-Contributed On Demand-4 Atomic-Precision Position Error Correction for Dopant-Array Quantum Devices*, James H.G. Owen, E. Fuchs, M. Haq, J. Randall,* Zyvex Labs

For dopant-based atomic-scale devices such as the 'single atom transistor' [1] and 2D Quantum Metamaterials[2], arrays of dopant patches need to be fabricated with atomic precision for both the size of the patches (to control the number of dopants in each patch) and the relative positioning of the patches in the array (to control the interactions between patches). As the number of patches scales up from a 3x3 array to a 32 x 32 array, this requires an automated writing process, without losing atomic precision patterning.

Various types of positioning errors are evident in the arrays. 'Staircasing' is the gradual upward drift of the boxes along each row, in alternating directions. 'Phase shift' is the misalignment of the boxes from one row to the next, which can reach a 180° phase shift. 'Curvature' or 'shearing' are distortions of the overall array shape. Various different sources of tip position error cause these distortions, including lattice lock misalignment, piezo creep and hysteresis, and thermal drift.

We are working to remove as many of these sources of imprecision as is possible, so as to achieve atomic precision dopant arrays of arbitrary size. Performing simulations of array fabrication which include deliberate errors of one type or another helps to isolate the source of the observed distortions, so that they can be corrected. 'Staircasing' is the result of drift, which can also affect the lattice lock, and therefore cause misalignment of the patterning with the lattice. 'Phase shift', however is indicative of xy creep. Shear and Curvature can be caused by uncorrected slow creep, or by variation in the rate of drift caused by temperature fluctuations in the lab.

By comparing the simulations with experimental data, we can determine which parameter, i.e. creep, hysteresis or drift correction, needs to be adjusted. We show that after adjustment we are able to draw arrays where the positioning errors are no more than 1 px.

Even with perfect positioning, the patches may not be the correct size due to sub-px position errors, stochastic errors such as tip changes, and incomplete lithography. We are working on machine-learning-based image recognition techniques to identify these defects, and correct them in an automated process.

In this way, we hope to be able to draw large arrays while maintaining atomic precision, which will enable Analog Quantum Simulations, and eventually 2D Quantum Metamaterials.

1: M. Fuechsle, J. A. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warschkow, L. C. L. Hollenberg, G. Klimeck, and M. Y. Simmons *Nat Nano***7** 242-246 (2012) DOI: 10.1038/nnano.2012.21

2: https://www.zyvexlabs.com/2d-workshop/workshop-overview/

Manufacturing Science and Technology Group
Room On Demand - Session MS-Invited On Demand

Manufacturing Science and Technology Invited On Demand Session

MS-Invited On Demand-1 Control of Plasma and Surface Reactions for Atomically Precise Device Fabrication*, Tetsuya Tatsumi,* Sony Semiconductor Solutions Corporation, Japan **INVITED**

According to the IRDS,[1] along with the progress of miniaturization in the future, technologies to control the processing at the atomic level to respond to new materials and new structures, including 3D stacked devices and new devices called Beyond CMOS, will be required. However, plasma and surface reactions are still often treated as black boxes in dry etching process control, and quantitative understanding and control of plasma processes will be more important for achieving high-precision processing. This paper briefly outlines the development history of dielectric film dry etching equipment and processes used to achieve high-precision processing characteristics and describes what is required for processing at the atomic layer level. In the 1980s and 90s, the development of a plasma sources with a high ion flux to increase the processing speed of SiO_2, and a process that strictly controlled the number of electron collisions ($\tau n_e<\sigma v>$) to suppress excessive dissociation of gas molecules to achieve high selectivity was established.[2] With the advent of low-k materials to realize high-speed, low-power devices, around 2000, a model for more delicate control of surface reactions and techniques for predicting incident flux have been proposed.[3] From 2010 onwards, techniques for predicting damage that cannot be observed with an electron microscope have been required.[4-5] Therefore, the energy distribution of incident ions and the penetration depth of high-energy particles have been quantitatively controlled. More recently, there have been active discussions about SiO_2 ALE.[6] In this process, however, since the reaction does not stop by self-limiting, it is necessary to predict and control the surface state when using plasma in the transient state before reaching the steady state.[7] In addition, latent defects[8] that cannot be recovered by heat treatment must be managed. We believe that technologies such as plasma monitoring, modeling, and prediction technologies will be further improved, and future atomic-level manufacturing technologies will be realized.

[1] https://irds.ieee.org/

[2] T. Tatsumi, et al., Jpn. J. Appl. Phys. 37, 2394 (1998).

[3] T. Tatsumi, et al., J. Vac. Sci. Technol. A23, 938 (2005).

[4] T. Kimura, et al., J. Vac. Sci. Technol. A23, 1068 (2007).

[5] Y. Nakamura., et al., J. Vac. Sci. Technol. A25, 1062 (2007).

[6] D. Metzler, et al., J. Vac. Sci. Technol. A 32, 020603 (2014).

[7] N. Kuboi, et al., J. Vac. Sci. Technol. A37, 051004 (2019).

[8] T. Kuyama, et al., Jpn. J. Appl. Phys. 59, SJJC02 (2020).

MS-Invited On Demand-13 Ion Tunable Electronic Materials Systems for Neuromorphic Computing*, Alec Talin,* Sandia National Laboratories **INVITED**

Tuning electronic conductance through solid state electrochemical ion insertion has emerged as a promising technology to enable next-generation, ultralow energy computing architectures[1-3]. Unlike two-terminal non-volatile memory elements, the three-terminal redox transistor decouples the 'write' and 'read' operations using a 'gate' electrode to tune the conductance state through charge transfer reactions involving ion injection into the channel electrode through a solid-state electrolyte. The insertion of ions into the bulk of the channel acts to dope the material through a gradual composition modulation that leads up to thousands of finely spaced conductance levels (synaptic weights) with near-ideal analog behavior. These properties enable low-energy operation without compromising analog performance and non-volatility. However, the strong coupling of ionic and electronic processes sharply challenges our current understanding of solid-state electrochemical systems, particularly at decreasing dimensions and timescales relevant to computing technology. In my talk I will discuss the rich portfolio of challenging, exciting fundamental science questions about ion tunable electronic materials systems and how we can harness these to realize a new paradigm for low power neuromorphic computing.

1. Fuller, E. J.;El Gabaly, F.;Leonard, F.;Agarwal, S.;Plimpton, S. J.;Jacobs-Gedrim, R. B.;James, C. D.;Marinella, M. J.; Talin, A. A., Li-Ion Synaptic Transistor for Low Power Analog Computing. *Advanced Materials* **2017,***29*.

2. Fuller, E. J.;Keene, S. T.;Melianas, A.;Wang, Z. R.;Agarwal, S.;Li, Y. Y.;Tuchman, Y.;James, C. D.;Marinella, M. J.;Yang, J. J.;Salleo, A.; Talin, A. A., Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing. *Science* **2019,***364* (6440), 570.

3. Li, Y. Y.;Fuller, E. J.;Asapu, S.;Agarwal, S.;Kurita, T.;Yang, J. J.; Talin, A. A., Low-Voltage, CMOS-Free Synaptic Memory Based on Li_xTiO_2 Redox Transistors. *Acs Applied Materials & Interfaces* **2019,***11* , 38982.

MS-Invited On Demand-19 Digital Electronics at the Atomic Scale*, Shashank Misra,* Sandia National Laboratories, USA **INVITED**

Tooling and development costs are poised to disrupt the microelectronics ecosystem, as they dramatically increase the risk in choosing a path to further shrink transistors from the nanoscale to the atomic scale. In this context, relaxing the requirement for achieving scalable manufacturing allows us to evaluate opportunities based on the physical limit of atoms, and not just based on incremental gains. Here, we examine progress in creating digital microelectronics using atomic precision advanced manufacturing (APAM), which uses a scanning tunneling microscope to pattern atomic resists at the surface of silicon with atomic precision, templating dopant precursor incorporation at the surface of silicon. By analogy, APAM functions as a pathway to area-selective doping.

For microelectronics, the value proposition for APAM devices is not in making single atom transistors that function at cryogenic temperatures. Rather, it derives from the ability to create atomically abrupt doping profiles whose density far exceeds the solid solubility limit, dramatically altering the electronic structure of silicon, and with more modest thermal budget requirements than ion implantation. These qualities motivate our re-evaluation of the vertical tunnel field effect transistor (TFET), whose long-promised energy efficiency compared to field effect transistors has been hindered by abruptness with which doping profiles can be defined. Despite this promise, APAM has mostly been used to fabricate simple “one-off” devices that function only at cryogenic temperatures. The first part of this talk will focus on our progress towards fabricating the first APAM-based TFET, including operating devices at room temperature and with a modern gate stack. The second part focuses on our work in establishing proofs-of-principle for manufacturability, including our efforts to directly integrate APAM into a CMOS manufacturing workflow and to extend APAM to volume wafer-scale fabrication at reduced lateral resolution. Along with the vertical TFET, the near-term application of reducing contact resistance in modern transistors only requires atomic precision in epitaxy as opposed to atomic precision laterally.

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MS-Invited On Demand-25 Extending Semiconductor Patterning Into the Next Decade*, Michael Lercel,* ASML **INVITED**

Scaling has enabled the semiconductor industry to be vibrant and growing for decades. Current market drivers continue to show a current and future strong demand for semiconductors. So the long term industry outlook is good – can technology keep up? Advanced patterning is dependent on having the right lithography, process, and metrology tools. Printing small features is not enough – tight control of tolerances, good yield, and cycle time are essential for manufacturability.

EUV is now positioned to enhance logic and memory processes with improved cycle time, less variability from multiple processes, and reduced process complexity compared to multiple patterning. Production with EUV is underway, so now the question becomes how does EUV enable the 3nm node and beyond.

EUV layer adoption is anticipated to increase at 5nm logic node versus the 7nm logic node where it is being first introduced. The same benefits of reduced process complexity, shorter cycle time, and reduced variability are now expanded as an all-optical 5nm logic node would involve nearly 100 mask levels. Beyond the 5nm logic node, higher Numerical Aperture (NA) EUV will further extend EUV single exposure resolution to enable Moore’s law scaling to the 3nm node and beyond.

In this presentation, we review the progress on enabling EUV for logic and memory manufacturing with progress on productivity, overlay performance, and availability of the EUV scanner plus the metrology and infrastructure progress to enable high-volume manufacturing. The extensions to enable EUV for 5nm node logic, and the preparation of high-NA EUV for 3nm and beyond node logic will be reviewed.

Author Index

Bold page numbers indicate presenter