III-V NanoWires for Junctionless Transistors Fabricated by Focused Ion Beam (FIB) System with Silicon Nitride Passivation

C. R. Almeida[1,2], P. L. Souza[3], M. P. Pires[4] and J. A. Diniz[1,2]
[1]School of Electrical and Computer Engineering, University of Campinas, 13083-852 Campinas, SP, Brazil
[2]Center for Semiconductor Components, University of Campinas, 13083-970 Campinas, SP, Brazil
[3]National Institute of Science and Technology of Semiconductor Nanodevices, PUC-Rio, 22451-900, Rio de Janeiro, RJ, Brazil
[4]Physics Institute, Federal University of Rio de Janeiro, 21945-970, Rio de Janeiro, RJ, Brazil
e-mail: cralmeid@gmail.com

III-V Junctionless semiconductors devices were fabricated on InGaP and GaAs substrates using Gallium (Ga^+) Focused Ion Beam (FIB) System. Two groups of samples, with n^+-InGaP (10nm)/GaAs-buffer layer (300nm) and n^+-GaAs (10nm)/GaAs-buffer layer (300nm), both on semi-insulating GaAs (001) nominal orientation substrates, were studied. The samples were grown by Metalorganic Vapor Phase Epitaxy (MOCVD) in an Aixtron AIX 200 horizontal reactor at 100mbar, where the samples are heated by infra-red (IR) lamps. The total hydrogen carrier gas flow rate was 8L/min. The precursors used for the GaAs growth were trimethylgallium (TMGa) and arsine (AsH_3). Silane (SiH_4) was used for the n doping. The layers were grown at 630°C with a growth rate of 0,36nm/s and a V/III ratio of 70 for the n doped layer. A pre-growth treatment for de-oxidation at 700°C was applied to the GaAs substrates for 15minutes under AsH_3 over pressure. Furthermore, for the first time, the silicon nitride layer (SiN_x), thickness of 10nm, deposited by ECR-CVD, was used as gate dielectric of Junctionless and as passivation layer of the surfaces of structures. The morphology of the samples was observed by Atomic Force Microscopy (AFM). X-Ray diffraction (XRD) analysis was used in order to determine the InGaP lattice parameter and mismatch to the GaAs substrate. Hall measurements provided silicon doping levels of $10^{+19}cm^{-3}$ for both groups of samples, indicating the formation of n^+-type layers. These samples were used for MOS Junctionless (JL) Transistors applications, since III-V semiconductors present higher electron mobility values than silicon. These JL transistors (with three terminals: gate, source and drain) are fabricated using a Focused Ion Beam (FIB) System. Thus, Gallium (Ga^+) Focused Ion Beam (FIB) is used to define the III-V (InGaP or GaAs) nanowires (III-V NWs), which are the electron conduction channel between source and drain and Pt deposition (as gate, drain and source electrodes) layers. Finally, drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and drain-source current (I_{DS}) versus gate-source voltage (V_{GS}) measurements of JL devices will be extracted and will be able to indicate if these InGaP or GaAs nanowires and the passivation, with the SiN_x deposited by ECR-CVD are of high quality and suitable for Junctionless technology.