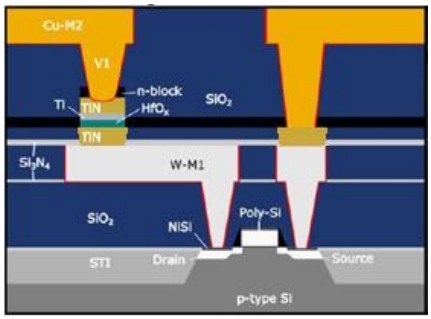

Fig.1: Schematic of CMOS-ReRAM integration.

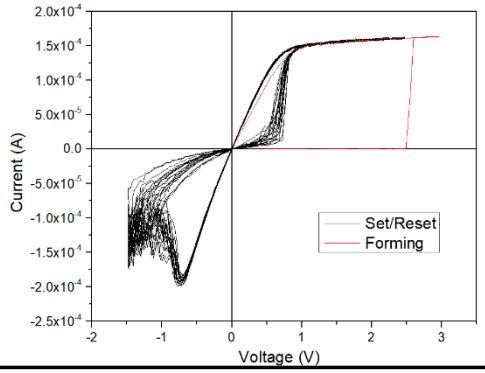

Fig. 2: Pulsed I-V sweeps showing forming, set and reset operation of RRAM device.

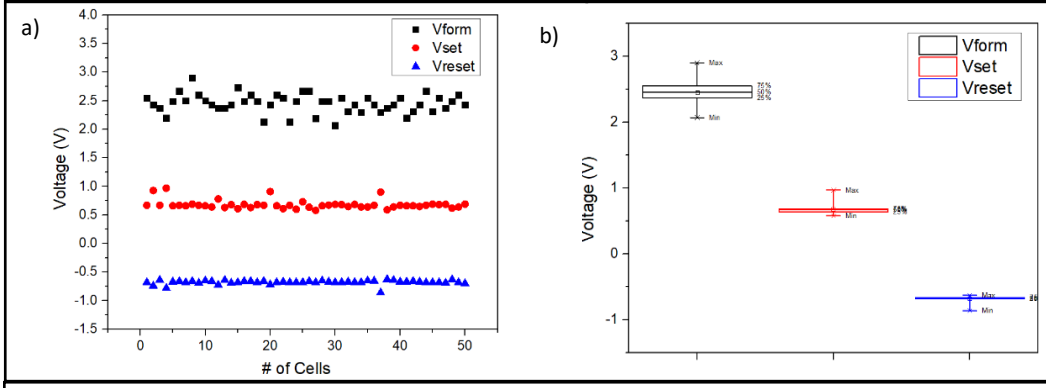

Fig. 3: a) Measured V_{form}, V_{set} and V_{reset} for 50 1T1R cells, and b) Statistical variation of those parameters showing min, max along with inter-quartile range of values for all cells.

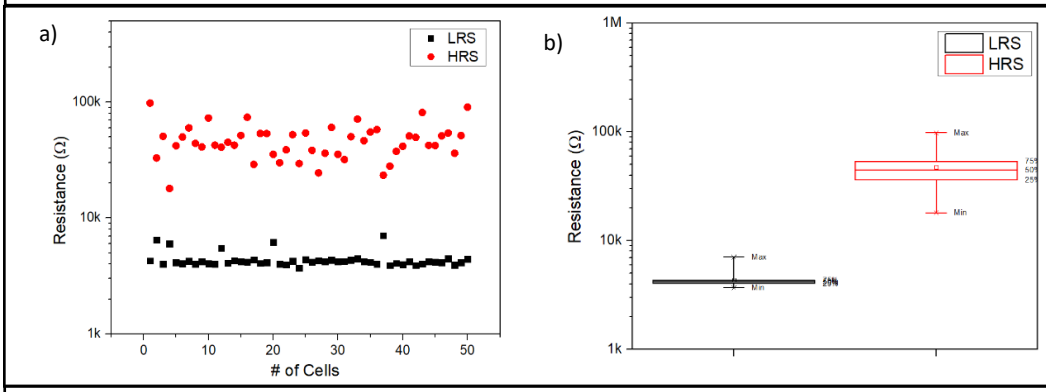

Fig. 4: a) Measured HRS and LRS for 50 1T1R cells, and b) Statistical variation of those parameters showing min, max along with inter-quartile range of all values for all cells tested.

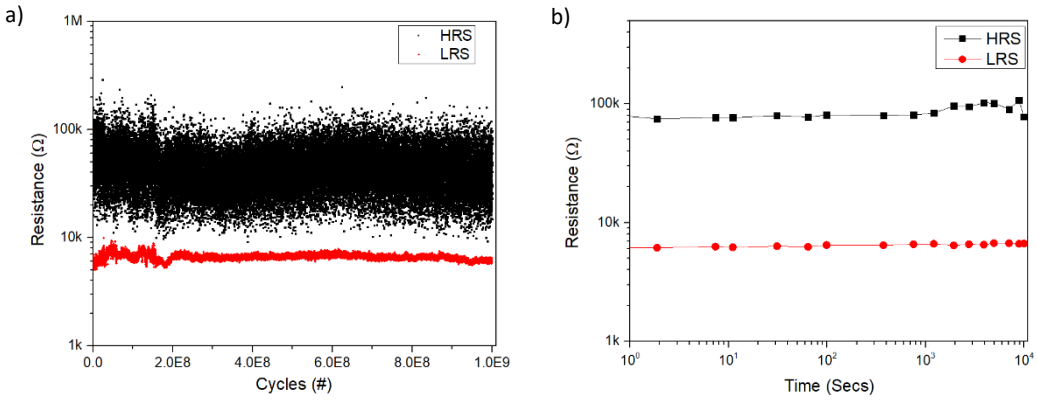

Fig. 5: a) Endurance measurement up to 1 billion switching cycles, and b) HRS and LRS retention up to 10^4 seconds at 100°C.

Table 1. Statistical analysis of RRAM Switching data for 50 1T1R cells.

Performance Metric	Mean	Std. Dev.
Avg. V_{form} (V)	2.45	0.16
Avg. V_{set} (V)	0.68	0.08
Avg. V_{reset} (V)	-0.678	0.037
Avg. LRS (Ω)	4.35 K	0.67 K
Avg. HRS (Ω)	47.4 K	16.35 K

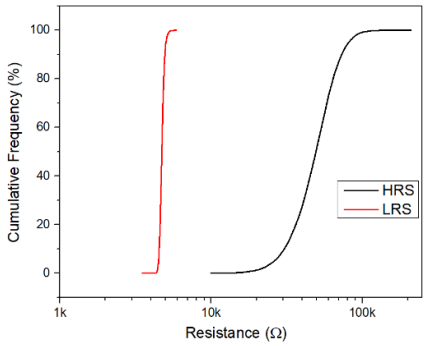

Fig. 6: Cumulative frequency distribution plot of LRS and HRS for fabricated HfO2 based RRAM devices.