HARDMASKS OF TiN AND Al FOR SILICON MICRO-CHANNEL DEFINITION VIA ICP PLASMA ETCHING PROCESS

C. S. Ruiz[1,2], A. R. Silva[1,2] , A. M. Rosa[2], J. A. Diniz [1,2],
*E-mail: camilasr@dsif.fee.unicamp.br
[1]School of Electrical and Computer Engineering (FEEC-UNICAMP)
Department of Semiconductors, Instruments and Photonic (DSIF)
[2]Center for Semiconductor Components (CCS_UNICAMP)
UNICAMP, 13083-970, P.O. Box. 6061, CAMPINAS, SP, Brazil.

ABSTRACT

TiN and Al films were used as hard mask (HM) materials in Si etching using a high-density inductively coupled plasma (ICP) reactor for silicon micro-channel (SiMC) (with depth > 1 µm) fabrication. The main proposal on this research is define a best hard mask (HM) for silicon micro-channel (SiMC) fabrication using ICP (Inductively Coupled Plasma) etching process. In addition, there are some important properties for hard mask should achieve, such as high mechanical performance and etch resistance to support the high process conditions. The TiN and Al films were deposited on silicon substrate (*p* type with (100) orientation) by sputtering. The TiN thickness was 100 nm, while two thickness values, 100 nm and 500 nm, were used for Al layers. The mask pattern, with parallel lines with width of 2 µm and spacing (between the lines) of 8 µm, was transfer on samples by lithography process and wet etching. To improve the adherence, some samples with both films were annealed at 450ºC for 10 minutes in forming gas ($92\%N_2+8\%H_2$) environment. Table 1 presents the obtained samples, with the thickness values and if the annealing was performed or not.

Table 1. The obtained samples and the Hard Mask (HM) conditions

Samples	HM	Thickness	Annealing
A	TiN	100nm	YES
B	TiN	100nm	NO
C	Al	100nm	YES
D	Al	100nm	NO
E	Al	500nm	YES
F	Al	500nm	NO

Table 2 The used ICP parameters
(fixed conditions: P=30mTorr, 450WICP, 100WRIE)

Process	ICP Parameters	Time (min)
#1	48sccmSF6+87sccmAr	10
#2	48sccmSF6+87sccmAr	20
#3	48sccmSF6+87sccmAr	30
#4	48sccmSF6+87sccmN2	10
#5	48sccmSF6+87sccmN2	20
#6	48sccmSF6+87sccmN2	30
#7	First sequence: 20seconds, 48sccmSF6+87sccmAr Second sequence: 20seconds,48sccmC3F8+87sccmAr	20
#8	First sequence: 20seconds, 48sccmSF6+87sccmN2 Second sequence: 20seconds,48sccmC3F8+87sccmN2	20

The ICP processes to fabricate the silicon micro-channels (SiMC) and to characterize the mask resistance under the plasma etching were carried out using these fixed parameters: 30 mTorr of process pressure, 450W of ICP and 100W of RIE (Reactive Ion Etching) powers. Two different gas mixtures were used for etching steps without the environment changing: 48sccm of SF_6 + 87sccm of Ar, and 48sccm of SF_6 + 87sccm of N_2. In these cases, three different times of 10, 20 and 30 minutes were employed. Two sequences of gas mixtures were used for etching steps in cycles with the gas environment changing: the first cycle was: 20 seconds with 48sccm of SF_6 + 87sccm of Ar, and in the sequence, 20 seconds, with 48sccm of C_3F_8 + 87sccm of Ar; the second cycle was: 20 seconds with 48sccm of SF_6 + 87sccm of N_2, and in the sequence, 20 seconds, with 48sccm of C_3F_8 + 87sccm of N_2. Both cycles were repeated until to complete the process time of 20 minutes. The steps in cycles with different gas environments were based on Bosch process [1,2], to get the silicon channels with depth up to 200 µm, with high aspect ratio. Usually, the Bosch process is performed using the cycles based on one sequence with SF_6/Ar gas mixture, to etch the silicon, and another, with C_4F_8/Ar, to passivate with the polymerization of the etched lateral walls. In this work, we have used C_3F_8 gas to polymerize the lateral walls, instead of traditional C_4F_8. Table 2 shows the conditions of ICP etching processes, which were performed to obtain the SiMC and to test the resistance of HM materials. The TiN hard masks, with or without annealing, have presented high resistance to etching process. However, the 100 nm Al films did not present high resistance, with or without annealing, mainly, when it is used plasmas with argon in the gas mixture, because the sputtering mechanism can occur. Only, the 500 nm thick layers (samples E and F, Table 1), with or without annealing, have presented the high resistance to etching process.

[1] F. Laermer , A. Urban,Microelectronic Engineering 67–68, 349–355, 2003
[2] M. Nunes., S.A. Moshkalev., C. Fischer., P.J.Tatsch., A. Flacker., The Electrochemical Society ECS Transactions, 23 (1)173-180, 10.1149/1,3183717, 2009.