Plasma Science and Technology Division
Room 104A - Session PS+EM+SE-TuM

Plasma Processing of Challenging Materials - I

Moderators: Necmi Biyikli, University of Connecticut, Jun-Chieh Wang, Applied Materials

8:00am **PS+EM+SE-TuM-1 Development and Understanding of Isotropic Etching Process of Si Selectively to $Si_{0.7}Ge_{0.3}$, *Sana Rachidi,*** *A Campo, V Loup,* CEA-LETI, France*; N Posseme,* CEA, LETI, France, France*; J Hartmann, S Barnola,* CEA-LETI, France

The vertically stacked wires MOSFET architecture pushes further the scaling limits of the CMOS technology. Now deemed as a possible extension to FinFET, it offers multiple benefits. A low IOFF current is indeed expected, thanks to multi-gate electrostatic control, with a high current drivability due to 3D vertically stacked channels.

The fabrication starts with the epitaxial growth of ($Si_{0.7}Ge_{0.3}$/Si) multilayers (8-12 nm for Si and SiGe layers) on blanket SOI substrates. Then, individual and dense arrays of fins were patterned to fabricate stacked-NWs FETs with 40 nm-pitch fins which are 36 nm high and roughly 20 nm wide. After that, dummy gates and spacers are defined prior to the anisotropic etching of the (Si/SiGe) multilayers. Today one of the most critical step in such device realization is the isotropic silicon removal selectively to silicon germanium.

In this study an understanding of selectivity evolution between Si and SiGe as a function of CF4/O2/N2 remote plasma parameters is presented. The experiments performed on 300mm blanket wafers (Si and $Si_{0.7}Ge_{0.3}$) have been carried out on CDE-Allegro.

The impact of etching parameters (CF_4, O_2, N_2, microwave-power, pressure and temperature of the electrostatic chuck) and different pre-treatments on etching rates and selectivity is first investigated. X-ray photoelectron spectroscopy (XPS) analyses will show that for Silicon, a SiO_xF_y thick reactive layer is formed on the etched surface and controls its etching regime. As for $Si_{0.7}Ge_{0.3}$, a passivation layer of 2 nm is observed. And it contains a mixture of GeO_x and SiO_xF_y species.

Based on these results, application to patterned wafers will be shown. Scanning Electron Microscopy (SEM), Transmission electron microscopy (TEM) and Energy Dispersive X-ray Spectroscopy (EDX or EDS) are here used for the pattern characterisation.

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8:20am **PS+EM+SE-TuM-2 III-V/Ge Heterostructure Etching for Through Cell Via Contact Multijunction Solar Cell*, Mathieu de Lafontaine,*** *G Gay, C Petit-Etienne, E Pargon,* LTM, Univ. Grenoble Alpes, CEA-LETI, France*; M Darnon, A Jaouad, M Volatier, S Fafard, V Aimez,* 3IT, Univ. de Sherbrooke, Canada

Through cell via contact architecture aims to increase the multijunction solar cell efficiency by 3% and the power yield per wafer by 20% by transferring the front side contact to the backside using insulated and metallized vias. Via hole plasma etching through the III-V/Ge heterostructure is a key step to fabricate this new architecture. It is challenging, as dozens of layers must be anisotropically etched with low roughness and free damage to ensure optimal cell performance. Moreover, etched patterns must have a depth of >30 µm and present >3 aspect ratio. In this abstract, several patterning strategies are presented to address these challenges.

The epiwafers consist of a 8µm-thick III-V heterostructure (InGaP, InGaAs, GaAs, AlInP, AlGaAs, AlGaInP layers and quantum dots) epitaxially grown on Ge substrate. A 5µm thick SiO_2 hard mask (HM) is first deposited by PECVD and patterned by contact photolithography and plasma etching. The optimization of both the lithography and HM opening steps is crucial for an optimal transfer into the III-V/Ge layers. It is observed that sloped and rough hard mask sidewalls after the HM opening step are detrimental to the via hole etching and lead to severe damage on the heterostructure sidewalls. Combining a thick photoresist mask with vertical sidewalls and an optimized $Ar/C_4F_8/O_2$ plasma process developed in a capacitive coupled plasma reactor allows to pattern the 5µm-thick HM with vertical and quite smooth sidewalls.

A room temperature $SiCl_4/Cl_2/H_2$ plasma process was developed in an inductively coupled plasma reactor to etch vias in the III-V/Ge heterostructures. The cell performance loss associated to via etching was almost absent, indicating that such chemistry is suitable for photovoltaic applications. However, some layers present isotropic etching, which is problematic for the via insulation and metallization. Indeed, III-V compounds with low indium concentration are more sensitive to lateral etching, thus creating preferential isotropic etching in several III-V layers. This represents a challenge considering the aspect ratio and the depth targets. Indeed, lateral etching will be even greater for a longer process time. To obtain anisotropic etching, a high temperature (200°C) $SiCl_4/Cl_2/H_2$ process is proposed. The enhanced volatility of the indium by-products combined with the Si-based passivation could improve the anisotropy while maintaining optimal cell performance. FIB-TEM and EDX are performed to characterize both the etch morphology and the passivation layer. Moreover, optoelectrical measurements will assess the cell performance after via etching.

8:40am **PS+EM+SE-TuM-3 Feature Scale Modeling of Etching of High Aspect Ratio Silicon Structures in Pulsed Plasmas*, Wei Tian,*** *J Wang, S Sadighi, J Kenny, S Rauf,* Applied Materials

As critical dimensions shrink below 7 nm, etching of high aspect ratio (HAR) Si structures, such as those used for shallow trench isolation (STI), is becoming challenging. Some strategies to deal with these challenges include multi-step cyclic processes and pulsed plasmas. In this paper, we consider a cyclic pulsed plasma process for Si etch. Etching is done by cycling three steps: oxidation (OX), Si main etch (ME) and clean. The OX step passivates the Si sidewalls and protects them during Si ME. Si is mainly etched during the ME step, where the ion energy and angular distribution (IEAD) and ion / neutral flux ratio are controlled through power pulsing. The clean step removes the Cl/Br-containing passivation from the Si surface prior to re-oxidation. Pulsed plasmas have demonstrated several advantages compared to continuous wave (CW) plasmas and have become indispensable in etching of the next generation of microelectronic devices [1-2]. When source power and/or bias power are pulsed, a variety of pulsing modes are possible. Pulsing duty cycles and phase shift provide additional knobs for controlling the etching characteristics. In order to understand the effects of pulsing modes on etching properties, a feature scale model coupled to a plasma model is desired.

In this work, we investigate several pulsing modes during the Si ME step including separate pulsing of the plasma source or bias powers, and their synchronized pulsing. Plasma models for the 3 steps including the pulsed plasma step [3] are coupled to a 3D Monte Carlo feature scale model. Process performance has been quantitatively evaluated by examining etch rates for Si and the SiO_2-like mask, Si/mask etch selectivity, and critical dimensions within the HAR features. When only the radio-frequency (RF) bias power is pulsed, Si and mask etch rates scale with pulse duty cycle. As a result, if Si is etched to the same depth, the HAR trenches are wider at higher duty cycles due to less total oxidation time and less protection of the sidewalls. Source power pulsing provides higher Si etch rate because of RF bias power being on continuously, but suffers from poor mask selectivity. Synchronized pulsing of both the source and RF bias powers in conjunction with phase control provides additional flexibility in modulating the IEAD and the ion/neutral flux ratio. RF bias pulsing and in-phase synchronized pulsing yield the best selectivity for the conditions explored.

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9:00am **PS+EM+SE-TuM-4 Plasma Etching of High Aspect Ratio Oxide-Nitride-Oxide Stacks*, S Huang, C Hurard,*** University of Michigan*; S Nam, S Shim, W Ko,* Samsung Electronics Co., Ltd., Republic of Korea*; **Mark Kushner,*** University of Michigan

Increasing demand for large memory capacity is now being met by 3-dimensional vertical structures. Fabricating these structures requires plasma etching through hundreds of stacked layers resulting in extremely high aspect ratio (up to 100) vias. The stack typically consists of alternately deposited silicon nitride and silicon oxide layers which serve as the sacrificial material and gate dielectric respectively. When combining the high aspect ratio (HAR) and hybrid materials, the etching of oxide-nitride-oxide (ONO) stacks faces both traditional (e.g., aspect ratio dependent etching, bowing and charging) and new challenges (e.g., mixing layers, line edge striation and tapered etch front through several layers).

In this paper, we report on results from a computational investigation of the etching of ONO stacks using tri-frequency capacitively coupled plasmas sustained in fluorocarbon gases. The reactor scale modeling was performed

using the Hybrid Plasma Equipment Model (HPEM), from which the neutral and ion fluxes and ion energy and angular distributions (IEADs) to the wafer surface were obtained. The feature scale modeling was performed using the 3-dimensional Monte Carlo Feature Profile Model (MCFPM) with a newly developed polymer mediated fluorocarbon etching mechanism for oxide and nitride.

During the etching of ONO stacks, the etch front quickly evolves to a tapered profile at low aspect ratio (~5) and persists into deeper features, mainly due to re-deposition of sputtered fluorocarbon radicals within the feature. The etch rate generally decreases with increasing aspect ratio due to limited transport of radicals and ions. Conductance, ion reflection from sidewalls and charging all play of role in the flux of reactive species to the etch front. When the etching proceeds through the ONO stack, the etch rate fluctuates, becoming higher for the nitride and lower for the oxide. The formation of scalloping due to different lateral etch rates for each material is observed for some conditions while not for others. The mechanism behind this scalloping, and methods to minimize its effect will be discussed.

* Work supported by Samsung Electronics Co. Ltd, National Science Foundation and the Department of Energy Office of Fusion Energy Sciences.

9:20am **PS+EM+SE-TuM-5 Etch Profile Evolution in Poly-silicon using Halogen Containing Plasmas for Next Generation Device Fabrication**, ***Shyam Sridhar**, S Voronin, P Biolsi, A Ranjan,* TEL Technology Center, America, LLC

The shrinking and introduction of complex three-dimensional device structures poses a great challenge for plasma etching. With ever-decreasing feature pitches, it is extremely important to achieve a near ideal etch profile, i.e. vertical sidewalls and flat etch fronts. The challenges are manifold in etching three-dimensional structures. For example, in etching high aspect ratio square shaped holes, it is difficult to remove the targeted material from the corners, especially at the bottom of the feature.

In this work, we report the impact of process parameters such as ion energy, neutral and ion fluxes on the profile evolution of closely spaced poly Si lines using F, Cl, and Br containing plasmas. Etching in Cl and Br plasmas resulted in anisotropic profiles with bowed and tapered sidewalls. Addition of gases such as oxygen or fluorocarbons to minimize bowing resulted in enhanced tapering of sidewalls. The etch fronts were found to be relatively flat or curved depending on the ion energy. Micro trenching was also found to influence the shape of the etch front. We attempt to extend the learning from etching two-dimensional lines to three-dimensional features, in order to define a better processing space for new and emerging applications.

9:40am **PS+EM+SE-TuM-6 Flux and Energy of Reactive Species Arriving at the Etch Front in High Aspect Ratio Features During Plasma Etching of SiO_2 in Ar/CF_4/CHF_3 Mixtures**, ***Soheila Mohades**,* University of Michigan*; M Wang, A Mosden,* TEL Technology Center America, LLC*; M Kushner,* University of Michigan

Multi-frequency, capacitively coupled plasmas (CCPs) provide additional control in semiconductor processing by separating production of ion fluxes from acceleration of ions into the wafer. In dual-frequency capacitively coupled plasmas (DF-CCPs), the higher frequency (HF, tens to hundreds of MHz) sustains the plasma and the lower frequency (LF, a few to 10 MHz) controls acceleration of ions into the wafer. Although the goal is to have completely separate control, changing the frequency and power of the LF does affect the magnitude of reactive fluxes to the wafer in addition to the ion energy and angular distributions (IEADs). As the aspect ratio (AR) of features approaches 100 in high aspect ratio (HAR) etching of dielectrics, the parameter of interest is the flux of reactants that reaches the etch front, which is not necessarily the same as the fluxes that enter the feature. Issues such as side-wall scattering and neutral conductance in the feature modify those fluxes as the AR increases.

In this paper, the IEADs and reactive fluxes reaching the etch front during fluorocarbon plasma etching of SiO_2 were computationally investigated as a function of AR. The feature scale modeling was performed using a 3-dimensional implementation of the Monte Carlo Feature Profile Model (MCFPM). The IEADs and reactive fluxes incident onto the feature were obtained using the 2-dimensional Hybrid Plasma Equipment Model (HPEM). The parameter space for the DF-CCP has LF of a few to 10 MHz, HF of 40 MHz, with powers of 100-1000 W applied to the bottom electrode with and without a dc-augmented top electrode in a gas mixture of Ar/CF_4/CHF_3 at 10s of mTorr. The reactive fluxes and energies onto the etch front for AR of up to 100 are discussed for ions, hot-neutrals and thermal neutrals.

* Work supported by TEL Technology Center, America, LLC, National Science Foundation and the Department of Energy Office of Fusion Energy Sciences.

11:00am **PS+EM+SE-TuM-10 Wafer-scale Fabrication of Suspended Graphene Nanoribbon Arrays -from Growth Dynamics to Optoelectrical Applications-**, ***Toshiaki Kato**, T Kaneko,* Tohoku University, Japan **INVITED**

Graphene nanoribbons (GNRs) combine the unique electronic and spin properties of graphene with a transport gap that arises from quantum confinement and edge effects. This makes them an attractive candidate material for the channels of next-generation transistors. However, the reliable site and alignment control of nanoribbons with high on/off current ratios remains a challenge. We have developed a new, simple, scalable method based on novel plasma catalytic reaction [1-5] for directly fabricating narrow GNRs devices with a clear transport gap [6]. Since the establishment of our novel GNR fabrication method, direct conversion of a Ni nanobar to a suspended GNR is now possible. Indeed, GNRs can be grown at any desired position on an insulating substrate without any post-growth treatment, and the wafer-scale synthesis of suspended GNR arrays with a very high yield (over 98%) is realized [7]. The growth dynamics of suspended GNR is also investigated through the systematic experimental study combined with molecular dynamics simulation and theoretical calculations for phase diagram analysis. The improvement of thermal stability of Ni nanobar can be a key to realize the GNR nucleation in our method, which can be given by supplying higher density of carbon from plasma to liquid-phase Ni nanobar. The wettability of liquid-phase Ni nanobar against to the SiO_2 substrate is also found to be an important factor forming the suspended structure of GNR. It is also revealed that the minimum length of GNR can be decided by the wavelength of Plateau-Rayleigh instability known as a traditional instability of fluid flow. We believe that our results can contribute to pushing the study of atomically thin layered materials from basic science into a new stage related to the optoelectrical applications [8-10] in industrial scale.

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11:40am **PS+EM+SE-TuM-12 Investigation of Surface Reactions for GeSbTe-based Phase Change Material: From Etching to Final Sealing Process**, ***Yann Canvel**, S Lagrasta,* STMicroelectronics, France*; C Boixaderas, S Barnola,* CEA-LETI, France*; E Martinez,* CEA/LETI-University Grenoble Alpes, France

Chalcogenide phase-change materials (PCMs), such as Ge-Sb-Te (GST) alloys, have shown outstanding properties, which have led to their successful use for a long time in optical memories (DVDs) and, recently, in non-volatile resistive memories. The latter, known as PCM memories, are among the most promising candidates to be integrated into next generation smart-power and automotive applications [1].

Chalcogenide PCMs exhibit fast and reversible phase transformations between crystalline and amorphous structures with very different resistivity states. This distinctive ability to store the information gives a unique set of features for PCMs, such as fast programming, flexible scalability, high data retention and performing endurance [2][3].

In the perspective of large-scale integration, which means incorporation of the PCM into more and more confined structures, the device performances are getting increasingly more sensitive to surface effects of the GST layer. Thus, it is crucial to maintain a homogeneous stoichiometric composition in the GST surface/volume all along the manufacturing process, particularly during the patterning of PCM cells.

In this study, we examine the main surface reactions that GST material must face and we illustrate how these reactions are likely to modify its composition.

In particular, we will focus on the surface damages generated by different halogen-based plasma etching processes [4][5]. An innovative etching method, compatible with extreme confined structures, will be highlighted.

Then, we will study the oxidation of GST, responsible of the critical surface degradation after the etching process [6]. According to the exposure conditions, the GST surface undergoes some specific chemical modifications that will be pointed out.

Finally, the stability of GST composition will be evaluated at each point of a standard GST patterning process: from etching to final sealing of PCM cells. It will allow us to understand how the chalcogenide material is degraded during the whole process. Some improvements will be exhibited in order to reduce this degradation.

Plasma etching were carried out in a 12 inch planar ICP reactor. And all the surface analyses were performed by using different techniques of material characterization, such as XPS, PP-TOFMS and EDS.

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12:00pm **PS+EM+SE-TuM-13 Behaviors of Charged Species in Afterglow of Dual Frequency Pulsed Capacitively Coupled Plasma with a Synchronous Negative DC-bias**, ***Takayoshi Tsutsumi,*** *T Ueyama, K Ishikawa, H Kondo, M Sekine,* Nagoya University, Japan*; Y Ohya,* Tokyo Electron Miyagi Limited*; M Hori,* Nagoya University, Japan

Dual frequency pulsed capacitively coupled plasma with a synchronous negative DC-bias to a top electrode is developed for the improvement of high-aspect-ratio contact hole (HARC) fabrications. It enables to suppress the distorted etched profiles such as twisting. These distortions are due to the distortions of ion trajectories inside the deep contact holes, which are charged up positively. It is expected that charged species presented in early afterglow were neutralized on the surfaces in the holes. we focus on the behavior of charged species in the afterglow period of the synchronous negative DC-bias imposition to the top electrode in the pulsed dual frequency CCP.

For temporal change of electron density in the afterglow, the synchronous negative DC-bias resulted in lower decay rate of electron density in afterglow[1]. The result indicate that higher DC-bias imposition causes more electron generation. Moreover, the decay rate near the bottom electrode is lower than that of near the top electrode. The possible explanation is electron generation or sustaining mechanism in the afterglow of DC synchronized pulsed plasma. We measured OES to confirm the electron generation or plasma sustainment in the afterglow. The intensities of Ar emission (at a wavelength of 750.38 nm) in afterglow decreased at the beginning of RF off period and increased after several μs. This phenomenon was not observed in the constant DC-bias condition.

The synchronous DC-bias voltage seems to accelerate the positive ions to the top electrode. And ion bombardment to the top electrode surface enhance the generation of the secondary electron in the afterglow. We consider that this influence the generation of negative ions and the neutralization of the charged surface of the hole in afterglow.

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Author Index

Bold page numbers indicate presenter