

## MEMS and NEMS Group

### Room 202B - Session MN+NS+PS-WeM

#### IoT Session: Multiscale Manufacturing: Enabling Materials and Processes

**Moderators:** Susan Burkett, The University of Alabama, Roya Maboudian, University of California at Berkeley

8:00am **MN+NS+PS-WeM-1 Miniaturizing 3D Printed Microfluidics: State-of-the-Art and Outlook**, *Greg Nordin*, Brigham Young University **INVITED**  
While there is great interest in 3D printing for microfluidic device fabrication, the challenge has been to achieve feature sizes that are in the truly microfluidic regime ( $<100\ \mu\text{m}$ ). The fundamental problem is that commercial tools and materials, which excel in many other application areas, have not been developed to address the unique needs of microfluidic device fabrication. Consequently, we have created our own stereolithographic 3D printer and materials that are specifically tailored to meet these needs. We show that flow channels as small as  $18\ \mu\text{m} \times 20\ \mu\text{m}$  can be reliably fabricated, as well as compact active elements such as valves and pumps. With these capabilities, we demonstrate highly integrated 3D printed microfluidic devices that measure only a few millimeters on a side, and that integrate separate chip-to-world interfaces through high density interconnects (up to 88 interconnects per square mm) that are directly 3D printed as part of a device chip. These advances open the door to 3D printing as a replacement for expensive cleanroom fabrication processes, with the additional advantage of fast (30 minute), parallel fabrication of many devices in a single print run due to their small size.

8:40am **MN+NS+PS-WeM-3 A Novel Inkjet Printing Technology Based on Plasma Conversion of Metal-Salt Based Inks for the Fabrication of Microfabricated Sensors**, *Y Sui, M Sankaran, Christian Zorman*, Case Western Reserve University

Inkjet printing is a leading additive manufacturing method to produce patterned metal thin films on flexible substrates. The most commonly-used inks consist of colloidal nanoparticle suspensions that employ organic molecules to stabilize the nanoparticles from agglomeration and precipitation. High temperature ( $>200^\circ\text{C}$ ) treatment is used after printing to remove the insulating organics and sinter the nanoparticles. The thermal step can limit printing on polymers such as PDMS, paper, and other temperature-sensitive substrates. Moreover the selection of metals is limited by those available in nanoparticle suspensions, with the most popular being Ag.

In this paper, we present the development of an ink-jet printing process that uses a particle-free, stabilizer-free ink and low-temperature plasma to produce electrically conductive metallic patterns on temperature-sensitive substrates. The inks are comprised of a metal salt, a solvent, and a viscosity modifier tailored to enable printing using a Dimatix DMP3000 series printer. The as-printed structures are treated with a low-pressure argon plasma which serves to convert the metal salt-based structures to metal structures with conductivities that approach bulk values. To date, we have demonstrated the process for Sn, Pb, Bi, Cu, Pt, Ag, Pd, and Au-based inks. The plasma-treated structures exhibit a high degree of porosity that can be as high as 70%, making them particularly well suited for use as active elements in microfabricated sensors. The extended paper will present details pertaining to the printing process, material characterization and testing of mechanical, chemical and biological sensors fabricated by this printing process.

9:00am **MN+NS+PS-WeM-4 Full Wafer Thickness Through Silicon Vias for MEMS Devices**, *Andrew Hollowell, E Baca, D Dagel, M Jordan, L Menk, K Musick, T Pluym, J McClain*, Sandia National Laboratories

A significant amount of development has been achieved integrating TSVs with standard silicon (Si) substrates; however, there are unique challenges associated with integrating TSVs with MEMS substrates. Industry has achieved TSV integration through a dependence on substrate thinning, a TSV reveal approach. However, often these MEMS devices depend on the thickness of the substrate for controlling the radius of curvature of the substrate, such as throughout Sandia's ultra-planar multilevel MEMS technology (SUMMIT™). TSV filling relies on tight control of the fluid kinetics during the electroplating process and the ability to balance the diffusion of  $\text{Cu}^{2+}$  and organic suppressor molecules throughout the depth of the via in order to realize a void-free fill of the TSV. In this work we have

extended the filling model for  $60\ \mu\text{m}$  deep TSVs, developed by Tom Moffat and Dan Josell, up to  $675\ \mu\text{m}$  deep TSVs.

In addition to the thickness constraints for MEMS integration, often MEMS devices are realized through unique release processes and are dependent on high temperature anneals. The most common release process is a hydrofluoric acid (HF) based release to selectively remove supporting oxide films and preserve the Si features that make up the MEMS components. The necessity to release structure in selective etchants presents additional challenges for integrating TSVs with MEMS components. We have overcome this challenge through the integration of additional capping layers which are selectively removed after the MEMS release. In order to accommodate the need for high temperature anneals we have removed the use of metal in the MEMS device and instead used doped silicon. The Cu TSVs are then integrated with the device after all the high temperature anneals are complete, making direct electrical contact to the doped Si. In this work, we present our integration approach for mating Cu TSVs with doped Si MEMS contacts and our plating approach for superfilling  $675\ \mu\text{m}$  deep,  $100\ \mu\text{m}$  wide TSVs.

This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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9:20am **MN+NS+PS-WeM-5 Scaling from Die Level to Full 150 mm Wafer TSV Filling through Fluid Dynamics Modeling and Current Controlled Deposition**, *Ehren Baca, M Jordan, L Menk, K Musick, P Yeh, A Hollowell*, Sandia National Laboratories

In this work we have developed a novel methanesulfonic acid (MSA) based electrolyte with a single suppressor additive for filling  $100\ \mu\text{m}$  diameter  $675\ \mu\text{m}$  deep through silicon vias (TSVs). Contrary to conventional three-additive systems we have achieved bottom up super filling of these large TSVs with a single suppressor additive. This bottom up super filling mechanism is dependent on a strict balance between applied potential and diffusion of both suppressor molecules and  $\text{Cu}^{2+}$  ions. The bottom up deposition was developed through die level plating experiments on sample sizes approximately  $1\ \text{in}^2$ . We control the solution replenishment by connecting the sample, both electrically and mechanically, to an aluminum rod and rotating the sample in solution. The rotation rate is directly correlated to the velocity of solution moving across the opening of the vias and therefore related to the solution replenishment inside the TSVs. At first a potentiostatic approach was used to supply a sufficient potential to break down the suppressor with a reference electrode in our plating cell.

Mapping the current, during deposition allowed us to develop a galvanostatic plating process.

Experiments were performed to scale this plating process to be compatible with production level electroplating tools. The fluid dynamics and applied current are significantly different on production plating tools. The tools do not come equipped with reference electrodes and in some cases, they have multiple anodes for current partitioning to control the uniformity of the electric field. Further, the wafer rotates about the center of the wafer and baffles are integrated into the tool to control the uniformity of a fountain type fluid replenishment system. With the wafer rotated about its center, there is a large variance in the velocity of fluid at different radii along the wafer. In this work, we present a set of scaling experiments performed on die with incremental increases in sample size to clearly map the die level plating parameters to a full wafer plating tool and achieve uniform TSV filling across a  $150\ \text{mm}$  wafer.

This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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# Wednesday Morning, October 24, 2018

9:40am **MN+NS+PS-WeM-6 Batch Level Electroless Under Bump Metallization for Singulated Semiconductor Die**, *Matthew Jordan, E Baca, J Pillars, C Michael, A Hollowell*, Sandia National Laboratories

Multi project-wafers (MPWs) allow multiple customers to share the cost of a manufacturing run from an advanced semiconductor foundry. This offers a cost-effective solution for low volume the fabrication or prototyping of application specific integrated circuits (ASICs). This practice is especially appealing for those in academia or government that often only require small quantities of devices for research or niche applications. With many products on a wafer, all the products must adhere to the same strict design rules. In practice this means that the final metallization is made using AlCu. This presents challenges for advanced packaging of MPW die as AlCu is not compatible with conventional flip chip solder because of oxidation of the AlCu metal. Further complicating the integration of MPW die is the fact that they are singulated prior to delivery, preventing the use of lithography, and thus ruling out the deposition and patterning of solder-compatible metals over the AlCu. This leaves the use of electroless plating schemes to prepare MPW die for 2.5D/3D die stacking.

We propose a batch process to facilitate MPW die processing through the electroless under bump metallization (UBM) process. This process includes passivation of the Si die sidewalls post dicing, MPW die mounting, batch Zn or Sn immersion followed by electroless Ni, electroless Pd, immersion Au (ENEPIG) or electroless Ni, immersion Au (ENIG) UBM deposition for reliable, UBM deposition. We have demonstrated 2.5D integration of batch processed, AlCu finished die that have UBM deposited using this process to an interposer using electroplated Cu pillars bumps and Au bumps.

Supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

11:00am **MN+NS+PS-WeM-10 MEMS-based Atomic Force Microscopy Probes: From Electromechanical to Optomechanical Vibrating Sensors**, *Bernard Legrand*, LAAS-CNRS, France; *L Schwab*, LAAS-CNRS, Univ Toulouse, France; *P Allain, I Favero*, MPQ, CNRS, Univ Paris Diderot, France; *M Faucher, D Théron*, IEMN, CNRS, Univ Lille, France; *B Walter*, Vmicro SAS, France; *J Salvétat*, CRPP, CNRS, Univ Bordeaux, France; *S Hentz, G Jourdan*, CEA-LETI, France

**INVITED**

Scanning probe microscopy has been one of the most important instrumental discoveries during the last quarter of the last century. In particular, atomic force microscopy (AFM) is a cross-disciplinary technique able to provide sample morphology down to the atomic scale. It offers invaluable tools to support the development of nano-sciences, information technologies, micro-nanotechnologies and nano-biology. For more than 20 years, boosting the scan rate of AFM has been an increasingly important challenge of the community. However still today, performing routine and user-friendly AFM experiments at video rate remains unreachable in most cases. The conventional AFM probe based on a micro-sized vibrating cantilever is the major obstacle in terms of bandwidth and resonance frequency.

Following a brief description of the context of the work, the talk will first describe the development of AFM probes based on MEMS devices that make use of ring-shaped microresonators vibrating above 10 MHz. A focus will be dedicated to the electrical detection scheme. Based on capacitive transduction and microwave reflectometry, it achieves a displacement resolution of  $10^{-15}$ m/VHz, allowing the measurement of the thermomechanical vibration of the MEMS AFM probes in air. Imaging capability obtained on DNA origamis samples at a frame rate greater than 1 image/s will be shown as well as investigation of block copolymer surfaces to elucidate the tip-surface interaction when vibration amplitudes are lower than 100 pm.

In the following, our recent research direction at the convergence of the fields of micro/nanosystems and VLSI optomechanics on silicon chips will be presented. Optomechanical resonators allow indeed overcoming the resolution limitation imposed by usual electromechanical transduction schemes. Here, we will introduce fully optically driven and sensed optomechanical AFM probes which resonance frequency is above 100 MHz and Brownian motion below  $10^{-16}$ m/VHz, paving the way for high-Speed

AFM operation with exquisite resolutions at sub-angstrom vibration amplitudes.

11:40am **MN+NS+PS-WeM-12 Suppressing Secondary Grain Growth in  $\text{Sc}_{0.125}\text{Al}_{0.875}\text{N}$  Using a CMOS Compatible Electrode**, *Giovanni Esteves, M Berg, M Henry, B Griffin, E Douglas*, Sandia National Laboratories

The electromechanical response of AlN can be enhanced by doping Sc into AlN up to ~43%. Challenges arise in processing high Sc doped AlN films due to the presence of secondary grain growth. Templating  $\text{ScAl}_{1-x}\text{N}$  (ScAlN) from a platinum bottom electrode has shown immense success in yielding highly textured *c*-axis ScAlN without the presence of secondary grain growth. However, platinum is not complementary metal-oxide-semiconductor (CMOS) compatible which makes it unattractive to those in industry. There is a need for a new bottom electrode that suppresses secondary grain growth while maintaining CMOS compatibility. In this work,  $\text{Sc}_{0.125}\text{Al}_{0.875}\text{N}$  and AlN films were grown on various underlying CMOS compatible metal stacks. Optimal film microstructure and texture was obtained for films deposited on highly textured {111} AlCu<sub>0.05</sub> bottom metal. AlN and ScAlN thicknesses were 750 nm and 850 nm and showed rocking curves of 0.81° and 1.09°, respectively. Atomic force microscopy was used to determine the presence of secondary grain growth and film roughness. The success of this bottom metal stack is attributed to lattice matching and low surface roughness which allows for highly oriented *c*-axis textured AlN and ScAlN. This work presents a metal stack that allows for the creation of higher Sc-doped AlN films while maintaining a high-quality microstructure and texture. Therefore, allowing for commercialization of Sc-doped AlN technologies which are capable of higher electromechanical coupling coefficients than AlN devices.

*This work was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.*

12:00pm **MN+NS+PS-WeM-13 A Low Voltage NEMS Relay. Design, Fabrication and Challenges**, *A Sopot, A Dinescu*, National Institute for R&D in Microtechnologies (IMT), Bucharest, Romania; *M Fernandez-Bolaños, A Ionescu*, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland; *Gina Adam*, National Institute for R&D in Microtechnologies (IMT Bucharest), Romania

Microelectromechanical switches (MEMS) have a wide variety of applications, such as in radio frequency switching, sensing, etc. thanks to their high non-linearity, sensitivity and integrability. Unfortunately, traditional MEMS typically need tens of volts for actuation, which prevents their use in applications that require low voltage CMOS circuitry. The typical size for MEMS switches is ~100µm, but recent work [1] has shown a scalable two-terminal nanoelectromechanical (NEMS) switch with low actuation voltage (<1V). The pipe clip structure is based on side edge actuation and is prone to reliability issues due to stiction since the electrode width is quite large (~300nm). We propose a structure based on a protrusion (dimple) small contact area and tunable dimensions during the fabrication process.

This paper presents a nanoelectromechanical switch with <3V actuation voltage. The proposed design is based on a fixed bottom electrode line (Pt) and two pillars that support a metallic nanowire (~100nm wide) beam line.

Since stiction is a significant issue for this device, the design includes protrusions (dimples) positioned in the center of the beam line with the scope of creating a small contact point with the bottom electrode. The structure is electrostatically actuated through a voltage applied on the beam while the fixed electrode is grounded. A small air gap between the beam and the bottom electrode line is crucial for reducing the actuation voltage, but can cause problems during the release. Finite element simulations in Comsol Multiphysics 5.2 were used to investigate the constraint space needed for the design of a NEMS relay with such a low actuation voltage, as needed for compatibility with a typical 3.3V CMOS technology. These simulations informed the geometries explored in the fabrication of a low power NEMS device with a double-clamped metallic beam. The surface micromachining process was developed to have a low-thermal budget (< 200 °C) and be multilayer CMOS compatible. The fabrication flow was based on SiO<sub>2</sub> as an inorganic sacrificial layer for

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obtaining a clean release. A mix of photolithography and e-beam lithography, lift-off and dry etching steps utilized are described, and challenges during the electrical characterization are discussed. Future design iterations focused on different beam designs are also presented.

J.O. Lee, Y.H. Song, M.W. Kim, M.H. Kang, J.S. Oh, H.H. Yang, and J.B. Yoon,  
"A sub-1-volt nanoelectromechanical switching device", *Nature nanotechnology*, 8(1), 36-40, 2013.

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