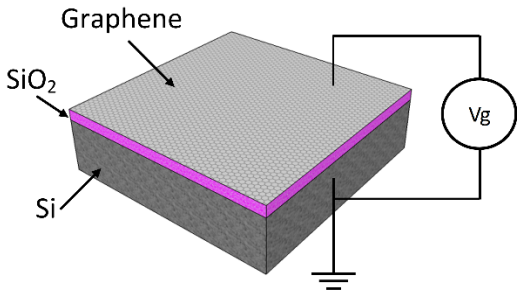

Figure 1. 3D schematic of a graphene/oxide/Silicon MOS device showing the applied gate voltage V_g.

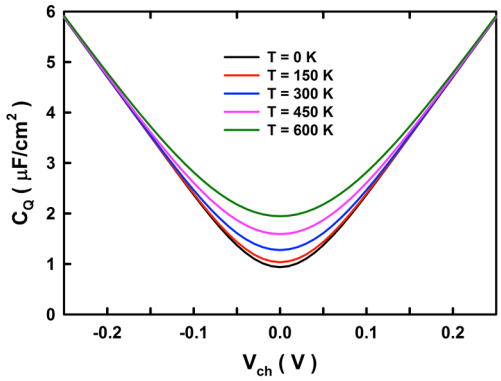

Figure 2. The numerically computed quantum capacitance of graphene in the presence of charged impurities C_Q as a function of the graphene electrostatic potential V_{ch} at different temperatures T.

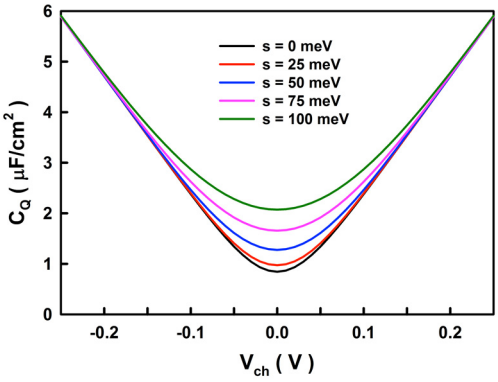

Figure 3. The numerically computed quantum capacitance of graphene in the presence of charged impurities C_Q as a function of the graphene electrostatic potential V_{ch} at different strengths of the potential energy fluctuations s.

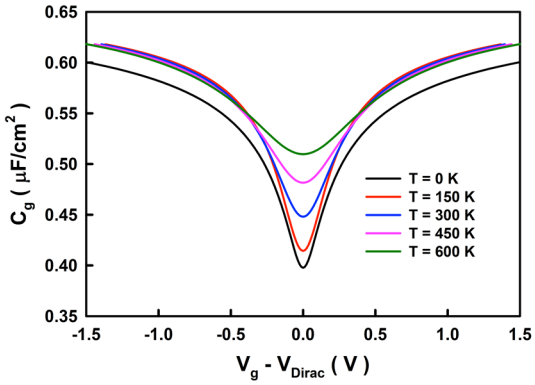

Figure 4. The numerically computed total gate capacitance C_g as a function of the gate voltage V_g at different temperatures T. V_{Dirac} denotes the Dirac voltage.

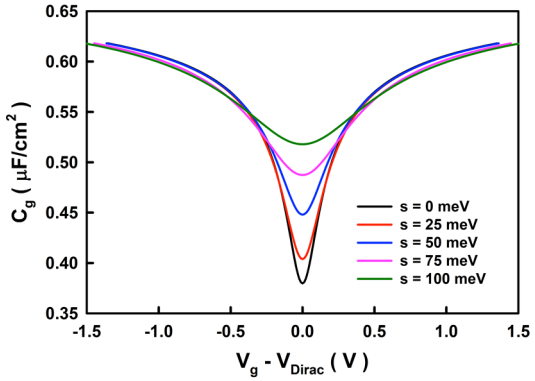

Figure 5. The numerically computed total gate capacitance C_g as a function of the gate voltage V_g at different strengths of the potential energy fluctuations s. V_{Dirac} denotes the Dirac voltage.

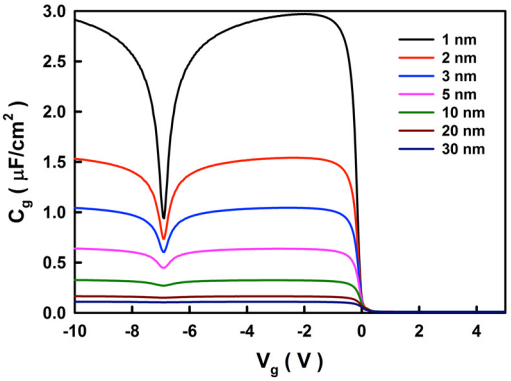

Figure 6. Full C_g-V_g curves of the graphene/oxide/Si MOS device at different equivalent oxide thicknesses ranging from 1 to 30 nm.