Plasma Science and Technology Division
Room 23 - Session PS-WeM
Advanced BEOL/Interconnect Etching

Moderators: Fred Roozeboom, TNO-Holst Centre & Eindhoven University of Technology, The Netherlands, GeunYoung Yeom, Sungkyunkwan University, Republic of Korea

8:00am **PS-WeM-1 Plasma Etch Considerations for EUV Quad-layer Patterning Stacks*, Angélique Raley*,** TEL Technology Center, America, LLC*; J Shearer, I Seshadri, A De Silva, J Arnold, N Felix,* IBM Research Division, Albany, NY*; H Cottle, A Metz,* TEL Technology Center, America, LLC

Continued scaling in semiconductor technology nodes has seen the rise of multi patterning for several critical layers, leading to higher costs, variability, and process complexity. EUV direct print patterning can alleviate and address some of these issues. The insertion of this technology was showcased in 2016[1] by the IBM Alliance for back end of the line (BEOL) metal trenches on their 7nm device. Exploratory efforts have now shifted to enabling the second generation of EUV patterning, targeting sub-36nm pitch resolution with single exposure. In current CAR-based EUV lithography, thin photoresist is used to prevent pattern collapse defectivity in dense line-space regions. This thin photoresist requires careful engineering of the hardmask and underlayer films below to minimize selectivity burden on etch budgets. This paper will first discuss the etch process design differences between current 36nm pitch EUV patterning and what is needed for sub-36nm pitch. Secondly, we will survey several thin hardmask materials and discuss their interactions with various plasma chemistries. For each material, the impact of both gas chemistry and tuning parameter on selectivity and resist roughness will be reviewed. Finally, continuous wave plasma etch performance will be contrasted with a quasi-ALE plasma etch process[1,2] as well as other plasma etch schemes designed to widen the patterning process window and enable successful pattern transfer into a typical BEOL metal patterning stack.

This work was performed by the Research Alliance Teams at various IBM Research Facilities

[1] Xie, VLSI, IEDM, p. 2-7, 2016

[2] Cottle et al. AVS 2016 Quasi-ALE Plasma Etching of EUV Photoresist for Contact Profile Control and PR Selectivity Improvement

[3] Vinayak et al. AVS 2014 Plasma Etch Considerations for Roughness Improvements during EUV and DSA Pattern Transfer using Mid Gap CCP

8:20am **PS-WeM-2 Direct Metal Etch Evaluation for Advanced Interconnect*, Sara Paolillo*,** *F Lazzarino, N Rassoul, D Wan, D Piumi, Z Tokei,* IMEC

For many decades, the semiconductor industry could follow Moore's law by introducing innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials. While industry is almost ready for high volume manufacturing of the 7nm technology node, new approaches are constantly being tested by research centers to enable further scaling down to the 5nm and 3nm technology nodes targeting respectively a metal pitch of about 32nm and 21nm. At such aggressive pitches, the effective resistivity of damascene Cu wires increases drastically due to both surface and grain boundary scattering but also due to the need of a Cu diffusion barrier that can't be scaled down. Besides the resistivity aspect, low-k damages induced by both plasma processing and barrier deposition contribute to the low reliability performance of damascene Cu interconnects.

In this context, alternative integration schemes exploiting direct metal etch technology and alternative metals like Ru have gained interest. A semi-damascene flow for instance can advantageously be used to overcome the aforementioned challenges. It consists of opening the vias into the low-k layer and filling them with a blanket metal deposition; connection are then created into the metal layer through direct etch. The empty trenches are finally either filled with low-k or used in an air gap configuration. This concept shows many advantages: it is suitable for a barrier-less integration, it prevents low-k damage and it allows for larger metal grain size. Regarding material selection, Cu is not a viable option considering the well-known difficulties in reactive dry Cu patterning. Ru is chosen as an alternative thanks to the ease with which it can be patterned using a conventional RIE process. Moreover, Ru line resistance is expected to go below Cu line resistance at CD below ~13nm, considering a line aspect ratio of 2. A further decrease in resistance can be expected with an increase in the Ru line aspect ratio.

In this work, we study the integration of Ru as a material for interconnect wires using a semi-damascene flow. Ru lines at 32nm pitch and with an aspect ratio of at least 2 are patterned using direct RIE targeting lines of 16nm and exploring a scaling extension down to 12nm. We will compare the electrical performances of Ru lines made from 3 different integration schemes. In one case, the patterns will be obtained using EUV single print lithography and in the other two cases, a 193i lithography will be employed defining the metal lines either from the spacers in the Anti Spacer Quadruple Patterning (ASQP) approach or from the tone inverted trenches in the SAQP approach.

8:40am **PS-WeM-3 Evolution of Dielectric Etchers*, Hiromasa Mochiki*,** Tokyo Electron Miyagi Limited, Japan **INVITED**

Plasma etchers have met stringent requirements of selectivity, profile, loading and uniformity to make shrinking of device dimensions possible. To that end, plasma etchers evolved from single frequency capacitively coupled plasma (CCP) to multiple frequency CCP, high density plasma (ICP, Microwave) and remote plasma sources. CCPs have been employed in dielectric etches due to it's ability to achieve high ion energies and low dissociation rate. Single frequency CCP evolved to CCP with magnetic enhancement and decoupled CCPs with high frequency on the top electrode or on the wafer. These knobs provided independent control plasma density and ion energy. Innovation in RF engineering enabled RF power to be split in different segments of electrodes to provide uniformity control and to eliminate standing wave effects. Recently, Direct Current Superposition (DCS) has been added to CCPs to alleviate differential charging, control C/F ratio in fluorocarbon plasmas and curing of resists. In addition to etching dielectric SiO2 and low-k materials, CCPs are employed in etching hard-mask etching process. For 7nm and beyond technology, the shrinking of critical dimensions (CD) without iso-dense loading is required. To meet this requirement, in-situ ALD + Etch is used. With Fusion of Etch and ALD, CD shrink with atomic precision for various patterns, without causing CD loading is achieved. In addition, uniformly control of the CD shrinkage amount across the wafer and Line Edge Roughness Improvement are demonstrated by ALD + Etch process. Process results will be presented to elucidate etch hardware evolution.

9:20am **PS-WeM-5 Etch Residue Formation and Growth on Patterned Porous Dielectrics: Angle-resolved XPS and Infrared Characterization*, QuocToan Le*,** *E Kesters, F Holsteyns,* IMEC, Belgium

Porous low-k dielectrics have been commonly used in micro- and nanotechnologies since the past decade. In back-end of line interconnect, the dielectric layer is typically patterned by dry etching through a photoresist or metal hard mask using fluorocarbon-containing plasmas, followed by electroplating of Cu inside the etched patterns. Residues are always formed during the pattern etching, regardless of the hard mask type.

This study focused on the types of residues generated during, and after, the plasma patterning of TiN hard mask/ porous low-k damascene stack. The porous dielectric s used in this study were CVD organosilicate glass (OSG) with target *k*-values of 2.2 and 2.55. Stacks of Si substrate/ OSG/SiO_2/TiN (from bottom to top) of 45 nm ½ pitch were prepared as test vehicles. Several methods commonly used for blanket surface characterization were applied for the patterned structure under study, including contact angle, Fourier transform Infrared spectroscopy (FTIR), and X-ray photoelectron spectroscopy (XPS). Using fluorocarbon-based dry etch plasma to pattern the OSG, for both 45 nm ½ pitch stacks, etch residues were detected on the TiN surface, dielectric sidewall and bottom (Figure 1, after aging, Supplemental document). The XPS F1s core-level spectra collected from the patterned OSG consisted of two main components: a sharp peak centered at ~684.6 eV corresponds to F-Ti bonds and the peak at higher binding energy (chemical shift ~3.9 eV) can be assigned to C-F bonds. In order to have further insight into the residue location, XPS spectra were collected at various take-off angles (TOA, measured with respect to the surface normal) with the beam perpendicular to the low-k lines. While the polymer-based residues (CFx) are mainly detected on trench sidewall and bottom (measured at low TOA, Figure 2, Supplemental document), the metal-based residues (TiFx) are mainly formed on the top surface (at high TOA). For the high binding energy component, the apparent chemical shift recorded at low and high TOA's is estimated to be ~0.85 eV, suggesting the presence of organometallic-type residues close to the top surface.

The effect of moisture and aging time on the density of the residues were investigated. Ti-containing residues tended to grow upon aging. The saturation level of the growth appeared to depend on the amount of the residues initially present on the surface. In terms of residue removal, the effect of a subsequent plasma treatment (post-etch treatment) and/or a wet clean on the removal of these residues was also studied.

9:40am **PS-WeM-6 Etch Challenges Associated with Sub-36nm Pitch BEOL EUV Patterning**, ***Jeffrey Shearer,*** IBM Research Division*; A Raley,* TEL Technology Center, America, LLC*; A De Silva, L Meli, I Seshadri, R Bonam, N Saulnier, B Briggs,* IBM Research Division*; T Oh,* Samsung Electronics Co. Ltd.*; A Metz,* TEL Technology Center, America, LLC*; J Arnold,* IBM Research Division

The rising cost of implementing EUV lithography is often cited as a major detractor for its adoption in future semiconductor technology nodes. The ability to directly print EUV levels with a single exposure not only alleviates some of the cost of processing but also many of the process challenges associated with multiple patterning techniques. However, scaling EUV technology, notably beyond 36nm pitch, comes with its own challenges. For example, constraints on resist thickness and hardmask material choices have emerged as unique etch challenges for BEOL patterning. Both new etch chemistries and novel etch techniques, such as the implementation of quasi-atomic layer etching and DC superposition, have proven invaluable in patterning beyond 36nm pitch.

We have demonstrated capability for EUV single exposure patterning beyond 36nm pitch using both trilayer and quadlayer patterning stacks. This paper will highlight benefits and challenges of each in terms of etch development. Specifically, SiARC-based patterning stacks will be compared to organic BARC-based quadlayer stacks with various hard layers in them. The introduction of each stack material was tested at 36nm pitch before transferring to sub-36nm pitch devices. Each pitch and stack has its own set of etch considerations, and we will address their impact on pattern transfer capability, CD process window, LER/LWR, the effort and methods necessary to overcome resist scumming, line end pullback, and others. An analysis of etch parameter selection will show how defectivity can be improved for each material stack. A programmed roughness structure allows detailed LER/LWR analysis for etch process tuning. Lastly, we will discuss the benefits and drawbacks of each patterning stack and present an outlook on material selection for next-generation sub-36nm pitch architecture.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

11:00am **PS-WeM-10 ALD-SiO2 Chamfer-Less-Flow for Dual Damascene Integration**, ***Xinghua Sun,*** *T Yamamura, A Metz, P Biolsi,* TEL Technology Center, America, LLC*; H Nagai, R Asako,* Tokyo Electron Limited PCDC, Japan

In the traditional back end of line (BEOL) Dual Damascene structure integration, all-in-one-etch flow has been widely applied for successful interlayer metal connection. As technical node is being scaled down to 10/7nm, ever 5nm with lower K value (2.5), via chain chamfer profiles become more and more important to chip yield. However, once via mask organic is stripped off during all-in-one etch, chamfer corner extensively exposes to trench etching plasma damage resulted from radical or ion bombardment. Therefore, chamfer corner can be etched much faster than trench, resulting in seriously rounded and chopped chamfer corner. In addition, ultra low K material can be damaged by some plasma like organic strip plasma. After the trench etch/wet clean and metallization, the rounded and chopped chamfer corner can cause electrical short, remarkably lowering yield and reliability. Regarding this point, it is a very critical goal to minimize such rounding/damage of chamfer as much as possible.

We here present an atomic layer deposition (ALD)-SiO2 chamfer-less Dual Damascene flow. In this flow, a few nanometer ALD-SiO2 film is deposited around via after via opening. The SiO2 pillar left on via sidewall plays the role to protect the chamfer corner from seriously chopping and damage while the following etching. According to different applications, this SiO2 pillar height is controllable and completely etched off while trench process. This can significantly improve the chamfer angle/profile. The ALD-SiO2 chamfer-less-flow has a few advantages. First, ALD oxide material can be uniformly deposited on via sidewall and easily etched off with trench process. Second, trench is not affected since the ALD-SiO2 is deposited before organic layer stripping. Third, it is a simple integration flow as only one extra SiO2 deposition step is added. The last one is to prevent electrical short between via chain and underneath metal, which improves the chip yield/reliability.

11:20am **PS-WeM-11 Tone Reversal Technology Development Targeting Below 5nm Technology Node Applications**, ***Stefan Decoster,*** *F Lazzarino, X Piao, N Rassoul,* IMEC, Belgium*; Y Fourprier,* TEL Technology Center, America, LLC*; D Piumi,* IMEC, Belgium

For many decades, the semiconductor industry could follow Moore's law by introducing innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials. While industry is almost ready for high volume manufacturing of the 7nm technology node, new approaches are constantly being tested by research centers to enable further scaling down to the 5nm technology node (N5) and below. In order to enable a number of these new integration approaches, there is a growing need for a well-understood and well-controlled tone reversal technology that consists of inverting the tonality of all structures present on the wafers, such as inverting ~20nm holes to blocks and sub-20nm lines to trenches, as well as large (micrometer-sized) structures such as alignment marks and overlay targets. The multiple Litho-Etch (LE) block patterning, the Self-Aligned Block (SAB) concept or the Direct Metal Etch (DME) approach are few examples of applications that advantageously integrate such tone reversal technology. A typical tone reversal flow consists of filling the patterns to be inverted with a material that could be either spin-coated or deposited. By means of dry etching or chemical mechanical polishing (CMP), the filling material is then thinned down to the top of the filled patterns which are finally selectively pulled out leaving the reversed patterns behind. A PECVD/ALD-type of filling would generally lead to the formation of voids between the patterns and to a low planarization performance requiring the use of an expensive CMP step that has a limited process window. Spin-coated materials are providing a good alternative to PECVD/ALD layers as they offer the possibility to achieve void-free filling and good planarization performance through material and process optimization. In this work, we focus on a fundamental understanding of the planarization properties of spin-coated materials. More specifically, the filling properties and planarization of different spin-coated materials (spin-on-glass, spin-on-carbon or spin-on-metal oxides) are screened in a selection of relevant matrix materials. By means of High Resolution Profiling, top-down and X-section Secondary Electron Microscopy the planarization properties are characterized as a function of pattern size, density and aspect ratio. Finally, the performances of the most promising tone reversal technologies are evaluated on concrete N5 and N3 applications like SAB and DME.

11:40am **PS-WeM-12 Towards the Elimination of Ultra-Low *k* Ash Damage Using an *In Situ*- Plasma Polymerized Film during Etch**, ***Katie Lutker,*** TEL Technology Center, America, LLC

Ultra-low-*k* SiCOH films (ULK) are commonly used as an interlayer dielectric layer in the back-end-of-line. Unfortunately, as the industry moves towards new lower-*k* materials, particularly for the 7 nm node and beyond, not only does the extent of the damage caused by ash to the ULK increase, but so does the effect of damaged material on device performance. Such damage can adversely alter the feature profile and CD, RC response, and device lifetime and because of the nature of the plasma etch can be difficult to prevent. The reduction or elimination of such ash damage would facilitate the continuation of in-situ ash during the dielectric open process while opening the door to more novel integration schemes that are currently limited by the creation of a damaged layer. In order to reduce the damage, we have developed a process to deposit a plasma polymerized organic film *in-situ*- during the etch process. The process utilizes a novel fluorine-free chemistry using a $C_xH_yN_z$ precursor to produce a conformal film -in an etch chamber. The deposition process was optimized using patterned substrates such that the effects of the plasma ash on the sidewalls and feature bottom could be monitored and compared. Because the deposition step occurs in the etch chamber, the deposition and etch steps can be cycled such that even the feature sidewalls are constantly protected. By tuning the deposition and subsequent ash plasma parameters, the resulting damage to the ULK was significantly reduced through the use of the protecting polymer film.

12:00pm **PS-WeM-13 Direct Metal Nanowire Patterning Using Ion Beam Etch**, ***Shreya Kundu,*** IMEC, Belgium*; S Dutta,* KU Leuven, IMEC, Belgium*; A Gupta, G Jamieson, D Piumi, J Boemmels, C Wilson, Z Tokei, C Adelmann,* IMEC, Belgium

Scaling of metal lines to sub-10 nm dimensions is a pivotal driving force for progressing in the field of electronics and physics. Their fabrication by conventional lift-off/damascene approaches can be highly demanding. Some of the challenges which need to be circumvented for their creation are high resolution lithography of thinner resist and pattern transfer to form well-resolved lines/spaces. In addition, stress induced ruptures can

form in the grain boundaries of the deposited metal film as the linewidth and grain size converge to similar dimensions. Here, we showcase an approach wherein we can directly pattern narrow metal lines with the use of relaxed dimension 248 nm optical lithography. Ru metal films of thicknesses ranging from 8-12 nm were deposited in a conformal way atop 300 nm wide (lines/spaces), ~7 µm long and 25 nm high patterned oxide (SiO_2) core. The oxide core height and the metal thickness can be varied to provide the flexibility of tuning the metal cross-sectional area. Ion beam etch (IBE) using Ar^+ ions was carried out to remove the film from the top and adjacent trenches of the oxide core, leaving behind long, continuous Ru lines of cross-sectional area <100 nm^2 along the oxide sidewalls. IBE works under the principle of physical momentum transfer (binary collision process) from the incident ions to the metal atoms which causes their eventual ejection from the substrate. Hence, unlike chemical etch, the physical etch process is not impacted by the change in grain size and grain boundaries of the metal. The cross-sectional area of the nanowires and its profile could be improved by controlling the Ar^+ ion accelerating voltage (50-400V) and time. TEM investigation revealed that the use of this ion bombardment based physical etch process didn't have an adverse impact on the metal crystallinity.

The Ru lines were electrically examined to estimate their performance as interconnects for advanced technology nodes. The electrical resistance yield achieved was >70%, indicating this physical etch process to be a robust method for such scientific studies. The fabrication method is not complex, compatible with the current silicon-based technology and can be extended to patterning of different metals and their alloys such as Ir, Rh amongst others.

References:

[1] L. G. Wen et al., ACS Appl. Mater. Interfaces, 2016, 8, 26119.

[2] S. Yasin, D. G. Hasko, H. Ahmed, Appl. Phys. Lett. 2001, 78, 2760.

[3] P. G. Glöersen, Journal of Vacuum Science & Technology 1975, 12, 28.

Author Index

Bold page numbers indicate presenter

— A —
Adelmann, C: PS-WeM-13, 2
Arnold, J: PS-WeM-1, 1; PS-WeM-6, 2
Asako, R: PS-WeM-10, 2
— B —
Biolsi, P: PS-WeM-10, 2
Boemmels, J: PS-WeM-13, 2
Bonam, R: PS-WeM-6, 2
Briggs, B: PS-WeM-6, 2
— C —
Cottle, H: PS-WeM-1, 1
— D —
De Silva, A: PS-WeM-1, 1; PS-WeM-6, 2
Decoster, S: PS-WeM-11, **2**
Dutta, S: PS-WeM-13, 2
— F —
Felix, N: PS-WeM-1, 1
Fourprier, Y: PS-WeM-11, 2
— G —
Gupta, A: PS-WeM-13, 2
— H —
Holsteyns, F: PS-WeM-5, 1
— J —
Jamieson, G: PS-WeM-13, 2
— K —
Kesters, E: PS-WeM-5, 1
Kundu, S: PS-WeM-13, **2**
— L —
Lazzarino, F: PS-WeM-11, 2; PS-WeM-2, 1
Le, Q: PS-WeM-5, **1**
Lutker, K: PS-WeM-12, **2**
— M —
Meli, L: PS-WeM-6, 2
Metz, A: PS-WeM-1, 1; PS-WeM-10, 2; PS-WeM-6, 2
Mochiki, H: PS-WeM-3, **1**
— N —
Nagai, H: PS-WeM-10, 2
— O —
Oh, T: PS-WeM-6, 2
— P —
Paolillo, S: PS-WeM-2, **1**
Piao, X: PS-WeM-11, 2
Piumi, D: PS-WeM-11, 2; PS-WeM-13, 2; PS-WeM-2, 1
— R —
Raley, A: PS-WeM-1, **1**; PS-WeM-6, 2
Rassoul, N: PS-WeM-11, 2; PS-WeM-2, 1
— S —
Saulnier, N: PS-WeM-6, 2
Seshadri, I: PS-WeM-1, 1; PS-WeM-6, 2
Shearer, J: PS-WeM-1, 1; PS-WeM-6, **2**
Sun, X: PS-WeM-10, **2**
— T —
Tokei, Z: PS-WeM-13, 2; PS-WeM-2, 1
— W —
Wan, D: PS-WeM-2, 1
Wilson, C: PS-WeM-13, 2
— Y —
Yamamura, T: PS-WeM-10, 2