Electronic Materials and Photonics Division
Room 14 - Session EM+SS-TuA
Surface and Interface Challenges in Semiconductor Materials and Devices

Moderator: Anthony Muscat, University of Arizona

2:20pm **EM+SS-TuA-1 Selective Atomic Layer Deposition of MoSi$_x$ -on Si (001) in Preference to Silicon Nitride and Silicon Oxide***, **JongYoun Choi**, C Ahles,* University of California, San Diego*; R Hung, N Kim,* Applied Materials, Inc.*; A Kummel,* University of California, San Diego

As MOSFETs size shrinks to <10 nm in a three dimensional structure (FinFET), electrical losses at the contacts must be minimized. Consequently, selective atomic layer deposition (ALD) of transition metal disilicides are of great interest due to their ability to minimize parasitic resistance and avoid lithograph onto a three dimensional structure. Selective ALD of metallic tungsten (W) via a fluorosilane elimination process have been demonstrated using WF$_6$ and SiH$_4$ or Si$_2$H$_6$.[1,2] This selectivity was achieved by an inherently favorable reactivity of the precursors on hydrogen-terminated Si versus OH-terminated SiO$_2$. In this W deposition process, SiH$_4$ was used as a reducing agent for W while the reactions byproducts was SiF$_4$. Here, we demonstrated that sub-stoichiometric silicide, MoSi$_x$ (x=0.4 – 1.1), can also be selectively deposited on H-terminated Si (001) in preference to SiOx and SiN using MoF$_6$ and Si$_2$H$_6$. X-ray photoelectron spectroscopy (XPS) was used to investigate the chemical composition of MoSi$_x$ ateach experimental step. It was observed that Si-H terminated silicon allowed single cycle nucleation of MoSi$_x$ at the substrate temperature of 100-120°C in contrast to an inherent chemical passivation (non-reactivity) on SiO$_x$ and SiN surfaces. To enable formation near stoichiometric MoSi$_x$, excess amount of Si$_2$H$_6$ was dosed after 5 ALD cycles to incorporate more Si into the MoSi$_x$ film while maintaining selectivity since the SiO$_x$ was unreactive to even high doses of Si$_2$H$_6$. This substrate-dependent selectivity was retained up to 5 - 10 ALD cycles. By applying a mixture gas of (H$_2$+MoF$_6$) instead of MoF$_6$ dosing, (as previous shown by Kalanyan et al[2]), the inherent selectivity was greatly improved and the nucleation of MoSi$_x$ was impeded up to at least 20 ALD cycles on SiN without perturbing MoSi$_x$ deposition on silicon. The growth rate of MoSi$_x$ on Si was ~0.8 Å/cycle; therefore, even 10 selective ALD cycles is sufficient for deposition of contacts. To confirm an *in-situ* selective deposition as well as the thickness of the film, MoSi$_x$ was deposited on a sample patterned with Si and SiON and the cross-section of the patterned sample was quantified using transmission electron microscopy (TEM). The surface morphology and roughness were measured using *ex-situ* atomic force microscopy (AFM) and *in-situ* scanning tunneling microscopy (STM). MoSi$_x$ on Si was conformal and atomically flat surface with root mean square (RMS) of 2.8 Å. Post-annealing in a ultra-high vacuum at 500°C for 3 mins further decreased the RMS roughness to 1.7 Å.

1. Thin Solid Films, **241**, 374 (1994)

2. Chem. Mater., **28**, 117-126 (2016)

3:00pm **EM+SS-TuA-3 Interface and Border Traps, their Passivation and the Reliability of Alumina Dielectric / Indium Gallium Arsenide Gate Stacks***, **Paul McIntyre**,* Stanford University **INVITED**

Both interface defects and border traps - charge traps in the gate oxide - influence the behavior of InGaAs metal-oxide-semiconductor (MOS) devices. This presentation will summarize the different effects of interface and border traps on the temperature- and bias-stress behavior of aluminum oxide/InGaAs MOS gate stacks, and will describe methods for passivating these defects both prior to and after gate dielectric deposition. The influence of local interface chemistry and the complex role of hydrogen as a defect passivant are highlighted.

In one set of experiments, a temperature dependent border trap response for Al$_2$O$_3$ gate dielectrics is investigated. This behavior is unexpected for defects that have typically been reported to charge and discharge through direct tunneling of electrons from the n-type substrate. Temperature dependent border trap frequency dispersion of the accumulation capacitance and conductance is found to be correlated with the presence of a defective interfacial layer, which can be intentionally produced either by excessive exposure to hydrating or oxidizing species during atomic layer deposition of Al$_2$O$_3$ or by use of a previously-reported aqueous HCl clean of the InGaAs surface prior to ALD. These results point out the sensitivity of the temperature dependence of the border trap response in metal oxide/III-V MOS gate stacks to the presence of processing-induced interface oxide layers, which alter the dynamics of carrier trapping at defects that are not located at the semiconductor interface.

We also report on the effects of pre- and post-atomic layer deposition (ALD) defect passivation with hydrogen on the trap density and reliability of Al$_2$O$_3$/InGaAs gate stacks. Reliability is characterized by capacitance-voltage hysteresis measurements on samples prepared using different fabrication procedures and having different initial trap densities. Despite its beneficial ability to passivate both interface and border traps, a final forming gas (H$_2$/N$_2$) anneal (FGA) step is found to induce a significant hysteresis. This is caused by hydrogen depassivation of defects in the gate stack under bias stress, supported by the observed bias stress-induced increase of interface trap density, and strong hydrogen isotope effects on the measured hysteresis. Additional strategies, beyond hydrogen annealing, for more stable interface defect passivation on InGaAs will be discussed briefly.

4:20pm **EM+SS-TuA-7 Controlling GaAs and Si Oxide Surface Energies***, **Karen L Kavanagh**,* Simon Fraser University, Canada*; N Herbots, A Brimhall, R Van Haren, Y Pershad, S Suhartono, E Landeros, R Culbertson,* Arizona State University*; R Islam,* Cactus Materials

Bonding two different semiconductors into a single integrated device can yield economic, medical, and human benefits by increasing performance. Si and GaAs bonding can increase solar cell efficiency and, if the bonding is hermetic, the lifetime of bonded sensors and optoelectronic circuits is extended by reducing percolation. Bonding occurs when the electronic properties of the two surfaces complement each other, to enhance efficient electron transfer.[1] Complementary surfaces can be identified through measurement of their total surface energy, γ^T, since this property can be modeled by Van Oss theory, to consist of three component interaction energies: molecular dipoles (Lifschitz-Van der Waals), γ^{LW}, electron donors, γ^-, and electron acceptors, γ^+. Measurements of the total and individual components of the surface energy of Si and GaAs (100) surfaces has been carried out using contact angle measurements of liquid drops with known surface energies, ranging from polar (18 MW water), apolar (α-bromo-naphthalene) to non-polar (glycerin). Accurate reproducible results are obtained using class 100 clean-room environments and analysis of multiple drops of each type of surface energy. This three liquid contact angle analysis (3LCAA) brings a much greater level of sophistication to this well-known and apparently-simple method. When carried out with semiconductor-level control of cleanliness, the contribution of each component to the total surface energy of Si (100) native and non-native oxides has been found to depend linearly on γ^{LW}. In hydrophobic oxide surfaces, γ^T is due almost entirely to molecular interactions, γ^{LW}, to within a few % error. Thus, the highly-passivated, thermally-grown SiO$_2$ surface with few defects or impurities, has a surface energy of 35.7 ± 3 mJ/m^2 that is entirely explained by γ^{LW}. However, γ^T can be raised to 57.3 ± 2 mJ/m$^{2.}$ by generating defects, and unsaturated or dangling bonds that interact with electron acceptors and or donors. This situation applies to heavily-etched, oxide surfaces, or chemically-oxidized surfaces. The contributions from $\gamma^-$and γ^+, raises the total surface energy γ^T up to 40% above that of γ^{LW}, which is found to remain nearly constant. Similar experiments with GaAs (100) surfaces as a function of surface preparation find that the Si-doped GaAs native oxide to be hydrophobic with a $\gamma^T$of 35 ± 3 mJ/m^2, with γ^{LW}contributing 98 ± 2%, thus close to the entirety of γ^T. This indicates a well-reacted native oxide. [1] *Herbots N. et al. US Patent 9,018,077 (2015); 9,589,801 (2017).*

4:40pm **EM+SS-TuA-8 *In Situ* Si$_3$N$_4$ Surface Layer on GaN-on-Si Heterostructure for High Power Operation***, **Chien-Fong Lo**, O Laboutin, X Gao, C Kao, H Marchand, W Johnson, R Pelzel,* IQE

Gallium nitride based devices have been delivering their promise of high power and high frequency operation as a capable replacement for silicon based devices, applications, owing to highly desirable III-nitride physical properties [1] . However, device performance is limited by excessive Schottky gate leakage, which results in high gate subthreshold leakage and leakage instability. These in turn cause high off-state drain leakage, a degradation of power efficiency, and ultimately device reliability problems.

Schottky leakage is caused by an excessive trap states density at the interface between the Schottky gate and the nitride semiconductor, resulting in excess negative charges on the barrier surface and/or in the barrier layer that induce current collapse in off-state operation. Dielectric capping of the III-nitride structure is one method to suppress the gate leakage in both forward and reverse bias, thereby mitigating current collapse and further improving the 3-terminal breakdown. Passivation with silicon nitride has been reported to reduce the current collapse and provide a relatively low state density at the SiN$_x$/III-N interface [2] and is widely used. However, in many instances, the SiN_x passivation is done *ex-situ* from the GaN epi system which results in an oxide layer at the nitride/SiN_x interface, which in turn reduces the efficacy of the passivation. Therefore, it is desirable to perform the SiN_x deposition *in-situ* so that the semiconductor/SiN_x interface is oxide-free.

In-situ, MOCVD SiN_x films have been grown on 100–200 mm Si substrates and characterized with RBS, AFM, XRD/XRR, and *C-V* profiling. Stoichiometric silicon nitride films with good surface morphology and material properties have been achieved. Metal-insulator-semiconductor HEMT (MISHEMT) devices with *in-situ* SiN_x capping layer were fabricated and compared with conventional GaN-capped HEMTs. Devices with *in-situ* passivation exhibit three orders of magnitude lower gate leakage current and improved 3-terminal breakdown (200V improvement at 10 µA/mm, see Fig. 1). Hall–Van der Pauw measurements performed on both GaN- and SiN_x-capped samples indicate that using *in-situ* SiN_x results in a significant increase in channel carrier density, which is consistent with SiN_x providing a reduced trap state density at the Schottky/semiconductor interface [3]. Additional electrical data including pulsed *I-V* will be presented to validate the improvements in switching performance. All of the nitride-based materials and SiN_x passivation layers have been grown using a commercial MOCVD reactor ensuring cost-effective implementation for commercial power-switching applications.

5:00pm **EM+SS-TuA-9 In-Vacuo Studies of Surface Structure and Surface Chemistry During Plasma-Assisted Atomic Layer Epitaxial Growth of InN Thin Films on GaN Substrates***, **Samantha Rosenberg**,* ASEE (residing at NRL)*; D Pennachio,* University California Santa Barbara*; V Anderson,* ASEE (residing at NRL)*; N Nepal,* U.S. Naval Research Laboratory*; C Wagenbach,* Boston University*; A Kozen,* ASEE (residing at NRL)*; Z Robinson,* SUNY Brockport*; J Logan, S Choi,* University California Santa Barbara*; J Hite,* US Naval Research Laboratory*; K Ludwig,* Boston University*; C Palmstrøm,* University California Santa Barbara*; C Eddy, Jr.,* U.S. Naval Research Laboratory

III-N semiconductors are well suited for applications in several important technological areas, including high current, normally-off power switches.[1-3] Such devices require heterostructures not readily achievable by conventional growth methods. While atomic layer deposition (ALD) is a versatile technique and has gained wide use, it does not offer the required level of crystallinity and purity for high-performance III-N semiconductor devices. Therefore, we have developed a technique adapted from ALD, called plasma-assisted atomic layer epitaxy (ALEp).[2]

Here we employ i*n-situ* and *in-vacuo* surface studies of GaN substrate preparation and InN ALEp growth to advance fundamental understanding of the ALEp process. We conduct *in-situ* grazing incidence small angle x-ray scattering (GISAXS) experiments at the Cornell High Energy Synchrotron Source, utilizing morphological evolution monitoring to investigate the growth interface during sample preparation at several different temperatures and film deposition at growth temperature. GISAXS information is complemented with *in-vacuo* x-ray photoelectron spectroscopy and reflection high-energy electron diffraction studies conducted at the Palmstrøm Lab at UCSB, where we consider traditional molecular beam gallium flash-off and atomic hydrogen etching as ways to produce the most suitable GaN surface for our ALEp-based approach.

1. N. Nepal, et al., Appl. Phys. Lett. 103, 082110 (2013)

2. C. R. Eddy, Jr, et al., J. Vac. Sci. Technol. A 31(5), 058501 (2013).

3. R. S. Pengelly, et al., IEEE Trans. Microwave Theory Tech. 60, 1764 (2012).

5:20pm **EM+SS-TuA-10 Aqueous Ammonium Sulfide Treatments on SiGe Surfaces***, **Stacy Heslop**, L Peckler, A Muscat,* University of Arizona

Employing germanium (Ge) and/or silicon germanium (SiGe) as the active material in transistors has the potential to generate electronics that are faster and consume less power. The narrower band gaps and higher hole mobilities compared to silicon make these materials ideal candidates for the next generation of microelectronics, but their integration into current manufacturing is difficult due to the rapid oxidation of germanium. These oxides are unstable, electrically defective, and form a poor interface with the underlying substrate hindering their electrical performance. The native GeO_2 is water soluble and unable to protect the surface during liquid phase processing. To combat this, the oxidation is prevented by depositing a thin sulfide layer to chemically passivate the surface. Ammonium sulfide is a common passivation reagent due to the size and valency of the sulfur atom and its ease of integration into current industrial processes. X-ray photoelectron spectroscopy (XPS) was used to study the effect of varying concentrations of aqueous ammonium sulfide on SiGe. No sulfide layer was detected for surfaces treated with aqueous ammonium sulfide and instead the surface reoxidized in solution. Hydrofluoric and hydrochloric acids were added to the ammonium sulfide solution to remove or prevent the formation of these oxides in solution. Samples treated with ammonium sulfide with added acid showed a sulfide layer. Increasing the concentration of HF and HCl increased the sulfur coverage but also increased the oxide coverage, suggesting the deposition of oxidized sulfur species.

Metal-insulator-semiconductor capacitors (MISCAPs) were fabricated for three different surface treatments. Capacitance –voltage and conductance data was used to quantify the density of interface defects (D_{it}). Samples treated with ammonium sulfide with added acid showed the highest sulfur coverage and had fewer interface defects (1.4×10^{12} cm^{-2} eV^{-1}) compared to samples treated with aqueous ammonium sulfide or samples with no sulfur treatment.

6:00pm **EM+SS-TuA-12 The Structural Stability and Phase Transition of $MoTe_2$ Activated by Thermal Annealing***, **Hui Zhu**, Q Wang, C Zhang, R Addou, K Cho, M Kim, R Wallace,* University of Texas at Dallas

Among group-VIB transitional-metal dichalcogenides (TMDs), semiconducting molybdenum ditelluride (2H-$MoTe_2$) with a similar bandgap to Si (~1.1 eV for monolayer and 1.0 eV for bulk state), is a promising candidate for electronic and photovoltaic applications.[1] Additionally, $MoTe_2$ possesses phase transition behavior, for example, the well-known phase transition between its semiconducting 2H structure and its semimetallic, distorted octahedral 1T' structure due to their small formation energy difference (~0.03 eV).[2] The thermally induced structural stability of $MoTe_2$ needs careful evaluation for nano-electronic device applications compared to the other TMDs due to a small electronegativity difference (~0.3) between Mo and Te, which may weaken the Mo-Te bonding strength. In this work, using scanning tunneling microscopy (STM), X-ray photoelectron spectroscopy (XPS), and scanning transmission electron microscopy (STEM), we investigated the thermal structural stability of $MoTe_2$ heated under high vacuum conditions and discovered an interesting decomposition or phase transition process from 2H-$MoTe_2$ (initial) to 2H-$MoTe_2$ surface decomposition with random Te atomic vacancies (200 °C and 300 °C) to semi-periodic, "wagon wheel" patterns of 60° inversion domain boundaries ($MoTe_{1.5}$ at boundaries, 400 °C) to one dimensional, metallic Mo_6Te_6 nanowires (NWs, 450 °C).[3] Particularly, the Mo_6Te_6 nanowires registered along the <11-20> 2H-$MoTe_2$ crystallographic directions with lengths in the micrometer range. The metallic NWs can act as an efficient hole injection layer on top of 2H-$MoTe_2$ due to the favorable band-alignment. Furthermore, an atomically sharp $MoTe_2$/Mo_6Te_6 interface and van der Waals gap with the 2H layers are preserved. The work highlights an alternative pathway for forming new transition metal chalcogenide phases and will enable future exploration of their intrinsic transportation properties.

This research was supported in part by the **SWAN** Center, a SRC center sponsored by the Nanoelectronics Research Initiative and NIST, and the Center for Low Energy Systems Technology, one of the six SRC STARnet Centers, sponsored by MARCO and DARPA.

Reference

(1) Keum, D. H.; et. al. Bandgap Opening in Few-Layered Monoclinic $MoTe_2$. *Nat. Phys.***2015**, *11*, 482–486.

(2) Cho, S.; et. al. Phase Patterning for Ohmic Homojunction Contact in $MoTe_2$. *Science.***2015**, *349*, 625–628.

(3) Zhu, H.; et. al. New Mo_6Te_6 Sub-Nanometer-Diameter Nanowire Phase from 2H-$MoTe_2$. *Adv. Mater.***2017**, 1606264.

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